everyday genius

MT6771 LTE-A Smartphone Application Processor Technical Brief

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Document Revision History

Revision	Date	Author	Description
0.1	2017-07-18	YT Lin	Initial draft
0.2	2017-09-20	YT Lin	Updated Figure 2-2, Table 2-36 and Table 2-37.
0.3	2017-12-05	MN Tsou	Updated features (LP4-3600 8GB/GPU 800MHz/connectivity).
1.0	2018-02-05	MN Tsou	1. Updated AVDD2_EMI/AVDDQ_EMI voltage for LP4. 2. Updated MSDC0 VIH and VIL.
1.1	2018-02-13	MN Tsou	Updated operation condition.

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1 System Overview

The MT6771 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE/LTE-A and C2K smart phone applications. The chip integrates ARM® Cortex-A73 operating up to 2.0GHz, ARM® Cortex-A53 operating up to 2.0GHz and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and UFS/MMC/SD cards.

The application processor, an Multi-core ARM® Cortex-A73, ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games.
All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

Imagination MIPS32® InterAptive, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 7, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE.

MT6771 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT6771 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT6771

- Quad-core ARM® Cortex-A73 MPCore™ operating at 2.0GHz
- Quad-core ARM® Cortex-A53 MPCore™ operating at 2.0GHz
- LPDDR3 up to 4GB (single channel with 32-bit data bus width)
- LPDDR4X up to 8GB (dual channels with 16-bit data bus width)
- Memory clock up to LPDDR3-1866 or LPDDR4-3600
- LTE Cat 7 (300Mbps)
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to FHD+ (2,400*1,080)
- OpenGL ES 3.0 3D graphic accelerator
- ISP supports 25MP@30fps
- HEVC 1080p @ 30fps decoder
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

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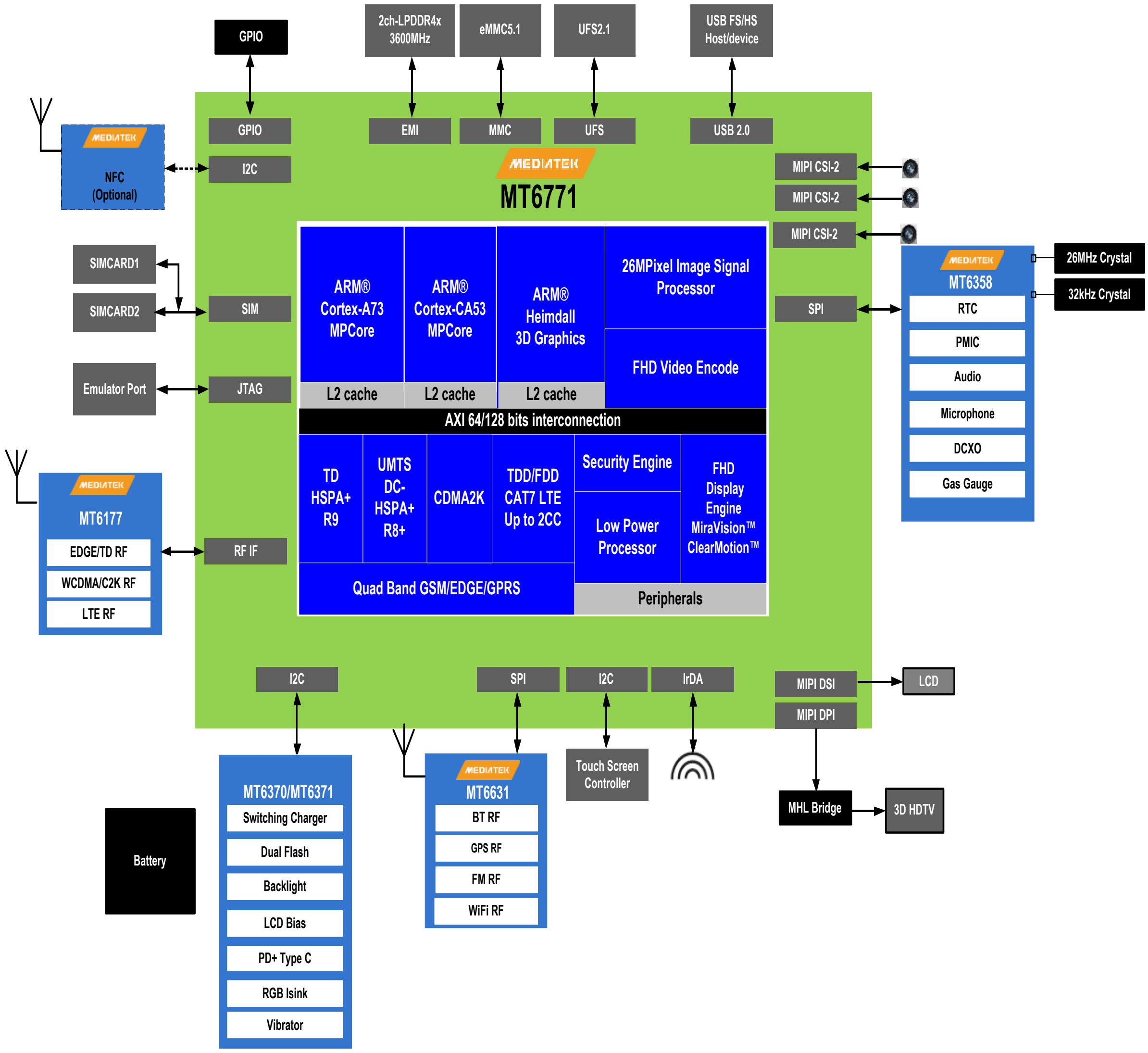

Figure 1-1. High-level MT6771 functional block diagram

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1.2 Platform Features

- **General**
  - Smartphone, two MCU subsystems architecture
  - Supports eMMC/uFS boot
  - Supports LPDDR3
  - Supports LPDDR4X

- **AP MCU subsystem**
  - Quad-core ARM® 2.0GHz Cortex-A73 MPCore™ with 64KB L1 I-cache, 64KB L1 D-cache and 1MB unified L2 cache
  - Quad-core ARM® 2.0GHz Cortex-A53 MPCore™ with 32KB L1 I-cache, 32KB L1 D-cache and 1MB unified L2 cache
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - DVFS technology with adaptive operating voltage from 0.6V to 0.95V

- **MD MCU subsystem**
  - Imagination MIPS32® InterAptive processor with max. 864MHz operation frequency
  - High-performance multi-core and multi-thread processor architecture (two cores and two threads)
  - 32KB L1 I-cache and 32KB L1 D-cache per core
  - 384KB SPRAM (Scratchpad memory, Two-Core's ISPRAM and DSPRAM)
  - 256KB L2 Cache (share L2 cache for two cores)
  - High-performance AXI bus Interfaces
  - Power management for clock gating control
  - FD216 DSP for running GSM modem with max. 312MHz operation frequency

- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security

- **External memory interface**
  - LPDDR3 up to 4GB (single channel with 32-bit data bus width)
  - LPDDR4X up to 8GB (dual channels with 16-bit data bus width)
  - Memory clock up to LPDDR3-1866 or LPDDR4X-3600
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB one port with USB3.0 device mode or USB2.0 OTG mode
  - eMMC5.1
  - uFS 2.1
  - 3 UART for debugging and applications
  - 6 SPI masters for external devices
  - 6 I2C/3 I3C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 3 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 2 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 0.7V/0.8V
  - I/O voltage: 1.8V/2.8V/3.3V

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  - Memory: 1.1V/0.6V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: VFBGA
  - 11.8mm*11.0mm
  - Height: Max. 0.9mm
  - Ball count: 599 balls
  - Ball pitch: 0.4mm

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1.3 Modem Features

- **LTE**
  - FDD/TDD Up to 300Mbps downlink, 150Mbps uplink
  - Downlink carrier aggregation (CA) ability; 1.4 to 20MHz RF bandwidth per component carrier (CC) and up to 2 CCs
  - 8*2 downlink SU-MIMO per component carrier
  - Downlink MU-MIMO per component carrier
  - Supports feICIC
  - Supports MBMS
  - Uplink CoMP ability
  - Advanced Interference Cancellation
  - Transmit Atenna Selection

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements
  - Transmit Atenna Selection

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection
  - Transmit Atenna Selection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12

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- Supports SAIC (Single Antenna Interference Cancellation) technology
- VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec
- Transmit Atenna Selection

- **CDMA2000 modem interfaces**
  - Supports CDMA2000 1xRTT (releases 0) and CDMA2000 HRPD/1xEV-DO Revision 0 and A
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link
  - Hybrid operation between 1x and HRPD
  - Simultaneous Hybrid Dual Receiver (SHDR) support
  - Supports 1x Diversity
  - Supports SRLTE
  - Transmit Atenna Selection

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1.4 Connectivity Features

The MT6771 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6631. With four advanced radio technologies integrated on one chip, MT6771/MT6631 is the best and most convenient connectivity solution in the industry, implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4 GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Supports single tri-band antenna for WLAN (2.4GHz and 5GHz), Bluetooth and GNSS
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)
- **Wi-Fi**
  - Dual-band (2.4/5GHz) single stream 802.11 a/b/g/n/ac MAC/BB/RF SoC, 20/40/80MHz bandwidth, MCS0~9 (256-QAM)
  - 802.11 d/e/h/i/j/k/r/v compliant
  - Security: WFA WPA/WPA2 personal, AES-CCMP, WPI-SMS4, GCMP, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: LDPC, STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports 802.11ac LDPC TX/RX, STBC TX/RX, 4T1R beamformee, MU-MIMO RX, WoWLAN
  - Supports MediaTek proprietary low power Green AP mode for portable hotspot operation
  - Auto rate control for optimizing the signal range and performance
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 23dBm CCK output power and 5GHz PA with max. 18.5dBm OFDM 54Mbps output power
  - RX sensitivity at 11n HT20 MCS7 mode and -62dBm 5GHz RX sensitivity at 11ac VHT80 MCS9 mode
  - Supports 32 multicast address filters and TCP/UDP/IP checksum offload
  - Per packet TX power control
- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance

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- Bluetooth v4.1+HS compliant
- Supports BT4.2
- PIP RX only, public indoor position (Direction Finding) (HW+FW+SW)
- AOD RX (for product) , AOA TX(test only)
- Integrated PA with 12dBm (class 1) transmit power
- Typical RX sensitivity with companion chip modem: GFSK -94dBm, DQPSK -95dBm, 8-DPSK -89dBm, BLE -96dBm
- Best-in-class BT/Wi-Fi coexistence performance
- Up to 4 piconets simultaneously with background inquiry/page scan
- Supports BT legacy, BLE scatternet
- Packet Loss Concealment (PLC) function for better voice quality
- Low-power scan function to reduce power consumption in scan modes
- Supports Wideband speech (16KHz sampling rate)
- SBC encode include mono and stereo
- SBC decode only support mono
- mSBC support in controller
- Supports secure connection with AES128 and ECC256
- Supports LTE coexistence enhanced features: Clock nudge and generalized interlace scan
- Supports FM over BT A2DP

- **ANT**
  - The wireless protocol standard for sport and fitness monitors
  - Supports different profiles for various applications: sport & fitness, health & Wellness, recreational activity, transportation, and information management etc.

- **GPS**
  - Supports GPS/Glonass/Beidou/Galileo/QZSS tri-band reception concurrently
    - GPS/Galileo only (GPS only)
    - GPS/Galileo - GLONASS (G+G)
    - GPS/Beidou (G+B)
    - GPS/GLONASS/Beidou (G+G+B)
    - GPS/Galileo/GLONASS (G+G+G)
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 8dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBµVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die

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- Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

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1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to FHD (2,400*1,080)
  - MIPI DSI interface (4 data lanes)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 8 overlay layers with per-pixel alpha channel and gamma table
  - Spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling

- **Graphics**
  - OpenGL ES 3.1/3.0/2.0/1.1 3D graphic accelerator capable of processing 2,400M pixel/sec @ 800MHz
  - OpenCL ES 1.1 full profile

- **Image**
  - Integrated image signal processor supports 32MP@30fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 25M sensors)
  - 3 MIPI CSI-2 high-speed camera serial interfaces; all are 4 data lane
  - PIP (picture in picture), [16MP + 16MP]@30fps
  - Hardware JPEG encoder: Baseline encoding with 200M pixel/sec. Continuous shot with 25M pixel@ 7fps
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - HEVC decoder 1080p @ 30fps/40Mbps
  - VP9 decoder 1080p @ 30fps/40Mbps
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - MPEG2 decoder 1080p @ 30fps/40Mbps
  - MPEG-4 encoder: Simple profile D1 @ 30fps
  - H.263 encoder: Simple profile D1 @ 30fps
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM

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- External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.
- 4-band IIR compensation filter to enhance loudspeaker responses
- Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
- Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
- Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

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2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

599	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	NC	EMI_EXTR	EMI0_DQ7		EMI0_DQ6		EMI0_CS1		EMI0_DQ11		EMI0_DQ12		EMI1_DQ10		EMI1_DQ13		EMI1_CA3		EMI1_DQ6		DVSS	UFS_RXO_RX		UFS_TXO_N		MSDC0_DAT	NC	A
B	WF_IP	AVDD18_W	EMI0_DQ4	EMI0_DMI0	EMI0_CA2	EMI0_CA3	EMI0_CA4		DVSS	EMI0_DQ10	EMI0_DQ8		DVSS	EMI1_DQ14	EMI1_DMI1		EMI1_CA2	EMI1_DMI0	EMI1_DQ5		DVSS	UFS_RXO_RX	DVSS	UFS_TXO_P	DVSS	MSDC0_DAT	MSDC0_DAT	B
C	WF_IN	AVDD12_W	DVSS	EMI0_DQS0	EMI0_DQ5	DVSS	EMI0_CA1	EMI0_DMI1	EMI0_DQ14	DVSS	DVSS	EMI1_DQ12	EMI1_DQ8	EMI1_DQ9	EMI1_CA1	EMI1_CS1	EMI1_CA4	DVSS	DVSS	EMI1_DQ4	EMI1_DQ7	AVDD09_UF	AVDD12_UF	DVSS	MSDC0_DAT	MSDC0_DAT	MSDC0_CM	C
D	WF_QP	WF_QN	DVSS	EMI0_DQS0	EMI0_DQ1	EMI0_DQ3	EMI0_CKE1	EMI0_CS0	EMI0_DQ13	EMI0_CK_T	EMI0_DQ15	DVSS		EMI1_DQ15	EMI1_DQ11	DVSS	EMI1_CA0	EMI1_CKE0	EMI1_CA5	EMI1_DQ2	DVSS	EMI_RESET_	AVDD18_UF	MSDC0_CLK	MSDC0_RST	MSDC0_DAT		D
E		DVSS	DVSS	DVSS	EMI0_DQ0	EMI0_DQ2	EMI0_CA5	EMI0_CKE0	EMI0_CA0	EMI0_CK_C	EMI0_DQ9	EMI0_DQS1	EMI1_DQS1	DVSS	DVSS	EMI1_CK_T	EMI1_CS0	EMI1_CKE1	EMI1_DQ3	EMI1_DQ1	EMI1_DQS0	UFS_RST_N		MSDC0_DAT	MSDC0_DSL	DVSS	DVDD18_M	E
F	BT_IN	BT_IP	DVSS	DVSS	DVSS				DVSS	DVSS	DVSS	EMI0_DQS1	EMI1_DQS1			EMI1_CK_C	DVSS	DVSS	DVSS	EMI1_DQ0	EMI1_DQS0		UFS_CKIN_2	DVDD_VQPS	AVDD33_US	USB_DM	AVDD18_US	F
G	BT_QP	BT_QN	DVSS	DVSS	DVSS	DVSS			AVDD18_D					AVDDQ_EMI	AVDDQ_EMI			AVDD2_EMI			DVSS		MSDC0_DAT	CHD_DM	CHD_DP	USB_DP		G
H		DVSS	CONN_HRST	CONN_BT_C	CONN_BT_D	CONN_WF_		XIN_WBG		AVDDQ_EMI	AVDD2_EMI	AVDDQ_EMI	AVDD2_EMI			AVDD2_EMI	AVDDQ_EMI		AVDDQ_EMI		DVDD_CORE	AVDD12_US	AVDD18_SS	DVSS	DVSS	DVSS	SSUSB_RXP	H
J	GPS_Q	GPS_I	DVSS	CONN_TOP_	CONN_TOP_	CONN_WF_	CONN_WF_	DVSS		DVSS	DVDD_CORE	DVDD_SRA	DVSS	EMI_TN	EMI_TP	DVDD_CORE	DVSS		DVDD_GPU	DVDD_GPU		AUD_DAT_	DVSS	SSUSB_TXN	SSUSB_TXP	DVSS	SSUSB_RXN	J
K			CAM_RST3	CAM_CLK2	CAM_RST2	CONN_WB_				DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVSS				PERIPHERAL	SYSRSTB	DVSS	DVSS	RTC32K_CK	AVDD09_SS	K
L	DVSS	DVDD18_IO	CAM_PDN3	CAM_CLK3	CAM_PDN2				DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVSS		DVDD_GPU			PERIPHERAL	AUD_DAT_	TESTMODE	PERIPHERAL	AUD_SYNC_		L
M	CSI1A_L0N	CSI1A_L0P	CSI1A_L1P	CSI1A_L1N	DVSS					DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVSS		DVDD_GPU		PERIPHERAL	WATCHDOG	AUD_CLK_	AUD_CLK_	AUD_SYNC_	DVDD18_IO	M
N	CSI1A_L2P	CSI1A_L2N	CSI1B_L0P	CSI1B_L0N	CSI0A_L2N_				DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVSS		DVDD_GPU		DVSS	PERIPHERAL	PWRAP_SPI	AUD_DAT_	SCP_VREQ_V	SCL6	AUD_DAT_	N
P	CSI1B_L1N	CSI1B_L1P	CSI0A_L0N_	CSI0A_L0P_	CSI0A_L2P_		DVDD_CORE			DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVSS		DVDD_GPU	DVDD_CORE	ANT_SEL0	PWRAP_SPI	PWRAP_SPI	PWRAP_SPI	SDA6		P
R	CSI0A_L1N_	CSI0A_L1P_	CSI0B_L0P_	CSI0B_L0N_	CSI2A_L1N		DVDD_CORE	DVDD_CORE	DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVSS		DVDD_GPU			ANT_SEL2	SRCLKENA0	SRCLKENA1	PERIPHERAL	DVSS	DSI0_D0N	R
T	CSI0B_L1N_	CSI0B_L1P_	CSI0B_L2P_	CSI0B_L2N_	CSI2A_L1P		DVDD_CORE	DVDD_CORE		DVSS	DVDD_SRA	DVDD_CORE		DVSS		DVDD_CORE		DVDD_SRA		DVDD_GPU	DVSS	PERIPHERAL	ANT_SEL1	DSI0_D3N	DSI0_D3P	DSI0_D1N	DSI0_D0P	T
U	CSI2A_L0N	CSI2A_L0P	CSI2A_L2N	CSI2A_L2P	DVSS		DVDD_PRO	DVDD_PRO	DVDD_PRO	DVDD_PRO			DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVDD_CORE		DVSS	DSI0_CKN	DSI0_CKP	DSI0_D1P		U
V	CSI2B_L0N	CSI2B_L0P	CSI2B_L1N	CSI2B_L1P	DVSS			DVSS	DVSS	DVSS		DVSS		DVSS		DVDD_CORE		DVSS		DVDD_CORE	DVDD_SRA	PERIPHERAL	AVDD12_DS	DSI0_D2N	DSI0_D2P	DVSS	AVDD04_DS	V
W	DVSS	SDA4	AVDD12_CS	EINT9	SRCLKENAI	CAM_PDN0	DVDD_SRA		DVDD_PRO		DVDD_PRO	DVSS	DVSS		DVDD_CORE		DVSS		DVDD_CORE		DVSS	SPI1_MI	DPI_D0	DPI_D6	DPI_D2	DPI_D3	DVDD18_IO	W
Y		SCL4		EINT10	CAM_PDN1	PERIPHERAL	PERIPHERAL	DVSS	DVSS	DVSS		TN_PLLGP1	TP_PLLGP1	DVSS	DVDD_SRA	DVDD_CORE		DVSS		DVDD_CORE		SPI1_MO	DPI_HSYNC	DPI_D7	PERIPHERAL	DPI_D9		Y
AA	DVDD18_IO	CAM_RST1	CAM_RST0	CAM_CLK0	KPROW0	PWM_A	PERIPHERAL			DVDD_PRO		DVSS	AVDD12_PL		DVDD_MOD		DVSS		DVDD_MOD		DVSS	SPI1_CLK	DPI_D11	DPI_VSYNC	DPI_D1	DPI_D10	DVDD18_M	AA
AB	SDA2	SCL2		EINT1	EINT0	SCL0	DVDD_CORE	DVSS	DVDD_PRO				AVDD18_PL	DVSS		DVDD_MOD		DVSS		DVDD_MOD	DVSS	DVDD_CORE	DPI_D5	DPI_D8	SPI1_CSB	DPI_D4	DVDD28_M	AB
AC		CAM_CLK1	EINT4	KPCOL0	SDA0	BPI_BUS0	AVDD18_CP		DVDD_PRO	DVDD_PRO	DVDD_PRO	DVSS	DVDD_SRA	DVDD_SRA	DVDD_MOD		DVSS		DVDD_MOD			DVDD_CORE	MSDC1_DAT	MSDC1_CLK	DPI_CK	DPI_DE		AC
AD	UTXD0	URXD0		EINT8	BPI_BUS5	MISC_BSI_C	DVDD_CORE	DVSS	DVDD_PRO	DVDD_PRO						DVDD_MOD			PERIPHERAL	I2S1_MCK	I2S1_LRCK	PERIPHERAL	SIM2_SCLK	MSDC1_DAT	PERIPHERAL	MSDC1_CM	MSDC1_DAT	AD
AE	EINT7	EINT6	KPCOL1	SCL1	BPI_BUS4	MISC_BSI_D	CDM5P5A			DVSS	RFIC_ETO_P	RFIC_ETO_N	APC	DVSS	DVSS	DVSS	MAIN_X26	AUXIN3	AUXIN2	RFIC0_BSI_	RFIC0_BSI_E	SIM1_SRST	SIM1_SCLK	SIM2_SIO	SIM2_SRST	MSDC1_DAT	DVDD28_SI	AE
AF		EINT5	SPI_CLK	SDA1	BPI_BUS3	MISC_BSI_C	CDM3P5A	DVSS	DVSS		TX_BB_IN1	TX_BB_QP1	TX_BB_IP0	TX_BB_QP0	DVSS	PRX_BB_I1	DRX_BB_Q	AUXIN1	AUXIN0	RFIC0_BSI_	RFIC0_BSI_C	SCL3	IDDIG	SIM1_SIO	DVDD28_SI	DRVBUS		AF
AG	EINT3	EINT2	SPI_CSB	BPI_PA_VM	BPI_BUS2	MISC_BSI_D	MISC_BSI_D	DVSS	DVSS		TX_BB_IP1	TX_BB_QN1	TX_BB_IN0	TX_BB_QN0	DVSS	PRX_BB_Q1	DRX_BB_I1	AUXIN4	I2S2_DI	RFIC0_BSI_	I2S1_DO	SDA3	I2S1_BCK	INT_SIM1	INT_SIM2	DSI_TE	DVDD18_SI	AG
AH	KPROW1	SPI_MO	BPI_PA_VM	BPI_OLAT0	BPI_BUS1	BPI_BUS7	MISC_BSI_C	DVSS	DVSS	DET_QP1	DET_IN1	DET_IP1	DET_QN0	DET_QP0	DVSS	DRX_BB_I0	DRX_BB_Q	DVSS	AVDD18_M	AVDD12_M	AVDD18_AP	BPI_BUS9	DISP_PWM	SCL5	SDA5	BPI_OLAT1	LCM_RST	AH
AJ	NC	SPI_MI		BPI_ANT1	BPI_BUS6		MISC_BSI_C	MISC_BSI_D	DVSS	DET_QN1		DET_IN0	DET_IP0		PRX_BB_Q0	PRX_BB_I0		REFP			DVDD18_IO	BPI_BUS10		BPI_ANT0	BPI_ANT2	BPI_BUS8	NC	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Figure 2-1. LPDDR4 ball map view

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599	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	NC	EMI_EXTR	EMI0_CA4		EMI0_CA6		EMI0_CS1		EMI0_DQ19		EMI0_DQ17		EMI0_DQ1		EMI0_DQ7		EMI0_DQ14		EMI0_DQ31		DVSS	UFS_RX0_RX		UFS_TX0_N		MSDC0_DAT	NC	A
B	WF_IP	AVDD18_WB	EMI0_CA7	NC	EMI0_CA3	NC	NC		DVSS	EMI0_DQ20	EMI0_DQ22		DVSS	EMI0_DQ3	EMI0_DMI0		EMI0_DQ15	EMI0_DMI3	EMI0_DQ28		DVSS	UFS_RX0_RX	DVSS	UFS_TX0_P	DVSS	MSDC0_DAT	MSDC0_DAT	B
C	WF_IN	AVDD12_WB	DVSS	NC	EMI0_CA2	DVSS	EMI0_CA1	EMI0_DMI2	EMI0_DQ16	DVSS	DVSS	EMI0_DQ0	EMI0_DQ2	EMI0_DQ4	EMI0_DQ8	NC	EMI0_DQ9	DVSS	DVSS	EMI0_DQ30	EMI0_DQ29	AVDD09_UF	AVDD12_UF	DVSS	MSDC0_DAT	MSDC0_DAT	MSDC0_CM	C
D	WF_QP	WF_QN	DVSS	NC	NC	EMI0_CA5	EMI0_CKE1	EMI0_CS0	EMI0_DQ18	EMI0_CK_T	EMI0_DQ21	DVSS		EMI0_DQ5	EMI0_DQ6	DVSS	EMI0_DQ11	EMI0_DQ10	EMI0_DQ13	EMI0_DQ24	DVSS	EMI_RESET_	AVDD18_UF	MSDC0_CLK	MSDC0_RST	MSDC0_DAT		D
E		DVSS	DVSS	DVSS	EMI0_CA9	EMI0_CA8	NC	EMI0_CKE0	EMI0_CA0	EMI0_CK_C	EMI0_DQ23	EMI0_DQS2_C	EMI0_DQS0_T	DVSS	DVSS	EMI0_DQS1_T	EMI0_DMI1	EMI0_DQ12	EMI0_DQ25	EMI0_DQ27	EMI0_DQS3_C	UFS_RST_N		MSDC0_DAT	MSDC0_DSL	DVSS	DVDD18_MS	E
F	BT_IN	BT_IP	DVSS	DVSS	DVSS				DVSS	DVSS	DVSS	EMI0_DQS2_T	EMI0_DQS0_C			EMI0_DQS1_C	DVSS	DVSS	DVSS	EMI0_DQ26	EMI0_DQS3_T		UFS_CKIN_2	DVDD_VQPS	AVDD33_US	USB_DM	AVDD18_US	F
G	BT_QP	BT_QN	DVSS	DVSS	DVSS	DVSS			AVDD18_DD					AVDDQ_EM	AVDDQ_EM			AVDD2_EMI			DVSS		MSDC0_DAT	CHD_DM	CHD_DP	USB_DP		G
H		DVSS	CONN_HRST	CONN_BT_C	CONN_BT_D	CONN_WF_		XIN_WBG		AVDDQ_EM	AVDD2_EMI	AVDDQ_EM	AVDD2_EMI			AVDD2_EMI	AVDDQ_EM		AVDDQ_EM		DVDD_COR	AVDD12_US	AVDD18_SS	DVSS	DVSS	DVSS	SSUSB_RXP	H
J	GPS_Q	GPS_I	DVSS	CONN_TOP_	CONN_TOP_	CONN_WF_	CONN_WF_	DVSS		DVSS	DVDD_COR	DVDD_SRA	DVSS	NC	EVREF	DVDD_COR	DVSS		DVDD_GPU	DVDD_GPU		AUD_DAT_	DVSS	SSUSB_TXN	SSUSB_TXP	DVSS	SSUSB_RXN	J
K			CAM_RST3	CAM_CLK2	CAM_RST2	CONN_WB_				DVSS		DVDD_COR		DVSS		DVDD_COR		DVSS				PERIPHERA	SYSRSTB	DVSS	DVSS	RTC32K_CK	AVDD09_SS	K
L	DVSS	DVDD18_IO	CAM_PDN3	CAM_CLK3	CAM_PDN2				DVSS		DVDD_COR		DVSS		DVDD_COR		DVSS		DVDD_GPU			PERIPHERA	AUD_DAT_	TESTMODE	PERIPHERA	AUD_SYNC		L
M	CSI1A_L0N	CSI1A_L0P	CSI1A_L1P	CSI1A_L1N	DVSS					DVSS		DVDD_COR		DVSS		DVDD_COR		DVSS		DVDD_GPU		PERIPHERA	WATCHDOG	AUD_CLK_	AUD_CLK_	AUD_SYNC	DVDD18_IO	M
N	CSI1A_L2P	CSI1A_L2N	CSI1B_L0P	CSI1B_L0N	CSI0A_L2N_				DVSS		DVDD_COR		DVSS		DVDD_COR		DVSS		DVDD_GPU		DVSS	PERIPHERA	PWRAP_SPI0	AUD_DAT_	SCP_VREQ_	SCL6	AUD_DAT_	N
P	CSI1B_L1N	CSI1B_L1P	CSI0A_L0N_	CSI0A_L0P_	CSI0A_L2P_		DVDD_COR			DVSS		DVDD_COR		DVSS		DVDD_COR		DVSS		DVDD_GPU	DVDD_COR	ANT_SEL0	PWRAP_SPI0	PWRAP_SPI0	PWRAP_SPI0	SDA6		P
R	CSI0A_L1N_	CSI0A_L1P_	CSI0B_L0P_	CSI0B_L0N_	CSI2A_L1N		DVDD_COR	DVDD_COR	DVSS		DVDD_COR		DVSS		DVDD_COR		DVSS		DVDD_GPU			ANT_SEL2	SRCLKENA	SRCLKENA	PERIPHERA	DVSS	DSI0_D0N	R
T	CSI0B_L1N_	CSI0B_L1P_	CSI0B_L2P_	CSI0B_L2N_	CSI2A_L1P		DVDD_COR	DVDD_COR		DVSS	DVDD_SRA	DVDD_COR		DVSS		DVDD_COR		DVDD_SRA		DVDD_GPU	DVSS	PERIPHERA	ANT_SEL1	DSI0_D3N	DSI0_D3P	DSI0_D1N	DSI0_D0P	T
U	CSI2A_L0N	CSI2A_L0P	CSI2A_L2N	CSI2A_L2P	DVSS		DVDD_PROC	DVDD_PROC	DVDD_PROC	DVDD_PROC			DVSS		DVDD_COR		DVSS		DVDD_COR		DVDD_COR		DVSS	DSI0_CKN	DSI0_CKP	DSI0_D1P		U
V	CSI2B_L0N	CSI2B_L0P	CSI2B_L1N	CSI2B_L1P	DVSS			DVSS	DVSS	DVSS		DVSS		DVSS		DVDD_COR		DVSS		DVDD_COR	DVDD_SRA	PERIPHERA	AVDD12_DS	DSI0_D2N	DSI0_D2P	DVSS	AVDD04_DS	V
W	DVSS	SDA4	AVDD12_CSI	EINT9	SRCLKENA	CAM_PDN0	DVDD_SRA		DVDD_PROC		DVDD_PROC	DVSS	DVSS		DVDD_COR		DVSS		DVDD_COR		DVSS	SPI1_MI	DPI_D0	DPI_D6	DPI_D2	DPI_D3	DVDD18_IO	W
Y		SCL4		EINT10	CAM_PDN1	PERIPHERA	PERIPHERA	DVSS	DVSS	DVSS		TN_PLLGP1	TP_PLLGP1	DVSS	DVDD_SRA	DVDD_COR		DVSS		DVDD_COR		SPI1_MO	DPI_HSYNC	DPI_D7	PERIPHERA	DPI_D9		Y
AA	DVDD18_IO	CAM_RST1	CAM_RST0	CAM_CLK0	KPROW0	PWM_A	PERIPHERA			DVDD_PROC		DVSS	AVDD12_PL		DVDD_MOD		DVSS		DVDD_MOD		DVSS	SPI1_CLK	DPI_D11	DPI_VSYNC	DPI_D1	DPI_D10	DVDD18_MS	AA
AB	SDA2	SCL2		EINT1	EINT0	SCL0	DVDD_COR	DVSS	DVDD_PROC				AVDD18_PL	DVSS		DVDD_MOD		DVSS		DVDD_MOD	DVSS	DVDD_COR	DPI_D5	DPI_D8	SPI1_CSB	DPI_D4	DVDD28_MS	AB
AC		CAM_CLK1	EINT4	KPCOL0	SDA0	BPI_BUS0	AVDD18_CP		DVDD_PROC	DVDD_PROC	DVDD_PROC	DVSS	DVDD_SRA	DVDD_SRA	DVDD_MOD		DVSS		DVDD_MOD			DVDD_COR	MSDC1_DAT	MSDC1_CLK	DPI_CK	DPI_DE		AC
AD	UTXD0	URXD0		EINT8	BPI_BUS5	MISC_BSI_C	DVDD_COR	DVSS	DVDD_PROC	DVDD_PROC						DVDD_MOD			PERIPHERA	I2S1_MCK	I2S1_LRCK	PERIPHERA	SIM2_SCLK	MSDC1_DAT	PERIPHERA	MSDC1_CM	MSDC1_DAT	AD
AE	EINT7	EINT6	KPCOL1	SCL1	BPI_BUS4	MISC_BSI_D	CDM5P5A			DVSS	RFIC_ET0_P	RFIC_ET0_N	APC	DVSS	DVSS	DVSS	MAIN_X26	AUXIN3	AUXIN2	RFIC0_BSI_	RFIC0_BSI_	SIM1_SRST	SIM1_SCLK	SIM2_SIO	SIM2_SRST	MSDC1_DAT	DVDD28_SI	AE
AF		EINT5	SPI_CLK	SDA1	BPI_BUS3	MISC_BSI_C	CDM3P5A	DVSS	DVSS		TX_BB_IN1	TX_BB_QP1	TX_BB_IP0	TX_BB_QP0	DVSS	PRX_BB_I1	DRX_BB_Q1	AUXIN1	AUXIN0	RFIC0_BSI_	RFIC0_BSI_	SCL3	IDDIG	SIM1_SIO	DVDD28_SI	DRVBUS		AF
AG	EINT3	EINT2	SPI_CSB	BPI_PA_VM	BPI_BUS2	MISC_BSI_D	MISC_BSI_D	DVSS	DVSS		TX_BB_IP1	TX_BB_QN1	TX_BB_IN0	TX_BB_QN0	DVSS	PRX_BB_Q1	DRX_BB_I1	AUXIN4	I2S2_DI	RFIC0_BSI_	I2S1_DO	SDA3	I2S1_BCK	INT_SIM1	INT_SIM2	DSI_TE	DVDD18_SI	AG
AH	KPROW1	SPI_MO	BPI_PA_VM	BPI_OLAT0	BPI_BUS1	BPI_BUS7	MISC_BSI_C	DVSS	DVSS	DET_QP1	DET_IN1	DET_IP1	DET_QN0	DET_QP0	DVSS	DRX_BB_I0	DRX_BB_Q0	DVSS	AVDD18_M	AVDD12_M	AVDD18_AP	BPI_BUS9	DISP_PWM	SCL5	SDA5	BPI_OLAT1	LCM_RST	AH
AJ	NC	SPI_MI		BPI_ANT1	BPI_BUS6		MISC_BSI_C	MISC_BSI_D	DVSS	DET_QN1		DET_IN0	DET_IP0		PRX_BB_Q0	PRX_BB_I0		REFP			DVDD18_IO	BPI_BUS10		BPI_ANT0	BPI_ANT2	BPI_BUS8	NC	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Figure 2-2. LPDDR3 ball map view

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2.1.2 Pin Coordinate

Table 2-1. Pin coordinate LPDDR4

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC_A1	K10	DVSS	AA2	CAM_RST1
A2	EMI_EXTR	K12	DVDD_CORE	AA3	CAM_RST0
A3	EMI0_DQ7	K14	DVSS	AA4	CAM_CLK0
A5	EMI0_DQ6	K16	DVDD_CORE	AA5	KPROW0
A7	EMI0_CS1	K18	DVSS	Y7	PERIPHERAL_EN10
A9	EMI0_DQ11	P22	ANT_SEL0	Y6	PERIPHERAL_EN11
A11	EMI0_DQ12	K23	SYSRSTB	W9	DVDD_PROC_L
A13	EMI1_DQ10	K24	DVSS	AA12	DVSS
A15	EMI1_DQ13	K25	DVSS	AA13	AVDD12_PLLGP
A17	EMI1_CA3	K26	RTC32K_CK	W11	DVDD_PROC_L
A19	EMI1_DQ6	K27	AVDD09_SSUSB	AA17	DVSS
A21	DVSS	L1	DVSS	J12	DVDD_SRAM_CORE
A22	UFS_RX0_RXP	P20	DVDD_GPU	AA21	DVSS
A24	UFS_TX0_N	L3	CAM_PDN3	AA22	SPI1_CLK
A26	MSDC0_DAT2	L4	CAM_CLK3	AD22	PERIPHERAL_EN12
A27	NC_A27	L5	CAM_PDN2	AD19	PERIPHERAL_EN13
B1	WF_IP	L9	DVSS	AA7	PERIPHERAL_EN14
B2	AVDD18_WBG	L11	DVDD_CORE	M22	PERIPHERAL_EN2
B3	EMI0_DQ4	L13	DVSS	T11	DVDD_SRAM_CORE
B4	EMI0_DMI0	L15	DVDD_CORE	AB1	SDA2
B5	EMI0_CA2	L17	DVSS	AB2	SCL2
B6	EMI0_CA3	R19	DVDD_GPU	AB4	EINT1
B7	EMI0_CA4	T23	ANT_SEL1	AB5	EINT0
B9	DVSS	L23	AUD_DAT_MISO1	AB6	SCL0
B10	EMI0_DQ10	L24	TESTMODE	AB7	DVDD_CORE
B11	EMI0_DQ8	R22	ANT_SEL2	AB8	DVSS
B13	DVSS	L26	AUD_SYNC_MOSI	V21	DVDD_SRAM_CORE
B14	EMI1_DQ14	M1	CSI1A_L0N	AB13	AVDD18_PLLGP
B15	EMI1_DMI1	M2	CSI1A_L0P	AB14	DVSS
B17	EMI1_CA2	M3	CSI1A_L1P	Y15	DVDD_SRAM_CORE
B18	EMI1_DMI0	M4	CSI1A_L1N	AB18	DVSS
B19	EMI1_DQ5	M5	DVSS	AC14	DVDD_SRAM_CORE
B21	DVSS	M10	DVSS	AB21	DVSS
B22	UFS_RX0_RXN	M12	DVDD_CORE	AB22	DVDD_CORE
B23	DVSS	M14	DVSS	L22	PERIPHERAL_EN3
B24	UFS_TX0_P	M16	DVDD_CORE	Y25	PERIPHERAL_EN4
B25	DVSS	M18	DVSS	AB25	SPI1_CSB
B26	MSDC0_DAT0	T20	DVDD_GPU	AD25	PERIPHERAL_EN5
B27	MSDC0_DAT1	AC25	DPI_CK	T18	DVDD_SRAM_GPU
C1	WF_IN	M23	WATCHDOG	AC2	CAM_CLK1

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C2	AVDD12_WBG	M24	AUD_CLK_MOSI	AC3	EINT4
C3	DVSS	M25	AUD_CLK_MISO	AC4	KPCOL0
C4	EMI0_DQS0_C	M26	AUD_SYNC_MISO	AC5	SDA0
C5	EMI0_DQ5	AA15	DVDD_MODEM	AC6	BPI_BUS0
C6	DVSS	N1	CSI1A_L2P	AC7	AVDD18_CPU
C7	EMI0_CA1	N2	CSI1A_L2N	AC13	DVDD_SRAM_PROC_B
C8	EMI0_DMI1	N3	CSI1B_L0P	W7	DVDD_SRAM_PROC_L
C9	EMI0_DQ14	N4	CSI1B_L0N	F24	DVDD_VQPS
C10	DVSS	N5	CSI0A_L2N_T1C	AC12	DVSS
C11	DVSS	N9	DVSS	AJ21	DVDD18_IOBL
C12	EMI1_DQ12	N11	DVDD_CORE	W27	DVDD18_IOLM
C13	EMI1_DQ8	N13	DVSS	M27	DVDD18_IOLT
C14	EMI1_DQ9	N15	DVDD_CORE	AC17	DVSS
C15	EMI1_CA1	N17	DVSS	AA1	DVDD18_IORB
C16	EMI1_CS1	AA19	DVDD_MODEM	AC22	DVDD_CORE
C17	EMI1_CA4	N21	DVSS	AC23	MSDC1_DAT2
C18	DVSS	W23	DPI_D0	AC24	MSDC1_CLK
C19	DVSS	N23	PWRAP_SPI0_CSN	N22	PERIPHERAL_EN6
C20	EMI1_DQ4	N24	AUD_DAT_MISO0	T22	PERIPHERAL_EN7
C21	EMI1_DQ7	N25	SCP_VREQ_VAO	AD1	UTXD0
C22	AVDD09_UFS	N26	SCL6	AD2	URXD0
C23	AVDD12_UFS	N27	AUD_DAT_MOSI1	AD4	EINT8
C24	DVSS	P1	CSI1B_L1N	AD5	BPI_BUS5
C25	MSDC0_DAT5	P2	CSI1B_L1P	AD6	MISC_BSI_CK_3
C26	MSDC0_DAT4	P3	CSI0A_L0N_T0B	AD7	DVDD_CORE
C27	MSDC0_CMD	P4	CSI0A_L0P_T0A	AD8	DVSS
D1	WF_QP	P5	CSI0A_L2P_T1B	L2	DVDD18_IORT
D2	WF_QN	P7	DVDD_CORE	E27	DVDD18_MSDC0
D3	DVSS	P10	DVSS	AA27	DVDD18_MSDC1
D4	EMI0_DQS0_T	P12	DVDD_CORE	K22	PERIPHERAL_EN8
D5	EMI0_DQ1	P14	DVSS	AD20	I2S1_MCK
D6	EMI0_DQ3	P16	DVDD_CORE	AD21	I2S1_LRCK
D7	EMI0_CKE1	P18	DVSS	V22	PERIPHERAL_EN9
D8	EMI0_CS0	AB16	DVDD_MODEM	AD23	SIM2_SCLK
D9	EMI0_DQ13	P21	DVDD_CORE	AD24	MSDC1_DAT0
D10	EMI0_CK_T	AA25	DPI_D1	AA6	PWM_A
D11	EMI0_DQ15	P23	PWRAP_SPI0_CK	AD26	MSDC1_CMD
D12	DVSS	P24	PWRAP_SPI0_MI	AD27	MSDC1_DAT3
D14	EMI1_DQ15	P25	PWRAP_SPI0_MO	AE1	EINT7
D15	EMI1_DQ11	P26	SDA6	AE2	EINT6
D16	DVSS	R1	CSI0A_L1N_T1A	AE3	KPCOL1
D17	EMI1_CA0	R2	CSI0A_L1P_T0C	AE4	SCL1
D18	EMI1_CKE0	R3	CSI0B_L0P_T0A	AE5	BPI_BUS4

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
D19	EMI1_CA5	R4	CSI0B_L0N_T0B	AE6	MISC_BSI_DO_3
D20	EMI1_DQ2	R5	CSI2A_L1N	AE7	CDM5P5A
D21	DVSS	R7	DVDD_CORE	AE10	DVSS
D22	EMI_RESET_N	R8	DVDD_CORE	AE11	RFIC_ET0_P
D23	AVDD18_UFS	R9	DVSS	AE12	RFIC_ET0_N
D24	MSDC0_CLK	R11	DVDD_CORE	AE13	APC
D25	MSDC0_RSTB	R13	DVSS	AE14	DVSS
D26	MSDC0_DAT7	R15	DVDD_CORE	AE15	DVSS
E2	DVSS	R17	DVSS	AE16	DVSS
E3	DVSS	AB20	DVDD_MODEM	AE17	MAIN_X26M_IN
E4	DVSS	AA26	DPI_D10	AE18	AUXIN3
E5	EMI0_DQ0	R23	SRCLKENA0	AE19	AUXIN2
E6	EMI0_DQ2	R24	SRCLKENA1	AE20	RFIC0_BSI_D1
E7	EMI0_CA5	AA23	DPI_D11	AE21	RFIC0_BSI_EN
E8	EMI0_CKE0	R26	DVSS	AE22	SIM1_SRST
E9	EMI0_CA0	R27	DSI0_D0N	AE23	SIM1_SCLK
E10	EMI0_CK_C	T1	CSI0B_L1N_T1A	AE24	SIM2_SIO
E11	EMI0_DQ9	T2	CSI0B_L1P_T0C	AE25	SIM2_SRST
E12	EMI0_DQS1_C	T3	CSI0B_L2P_T1B	AE26	MSDC1_DAT1
E13	EMI1_DQS1_T	T4	CSI0B_L2N_T1C	AG27	DVDD18_SIM
E14	DVSS	T5	CSI2A_L1P	AF2	EINT5
E15	DVSS	T7	DVDD_CORE	AF3	SPI_CLK
E16	EMI1_CK_T	T8	DVDD_CORE	AF4	SDA1
E17	EMI1_CS0	T10	DVSS	AF5	BPI_BUS3
E18	EMI1_CKE1	AC15	DVDD_MODEM	AF6	MISC_BSI_CK_2
E19	EMI1_DQ3	T12	DVDD_CORE	AF7	CDM3P5A
E20	EMI1_DQ1	T14	DVSS	AF8	DVSS
E21	EMI1_DQS0_C	T16	DVDD_CORE	AF9	DVSS
E22	UFS_RST_N	AC19	DVDD_MODEM	AF11	TX_BB_IN1
E24	MSDC0_DAT3	AD16	DVDD_MODEM	AF12	TX_BB_QP1
E25	MSDC0_DSL	T21	DVSS	AF13	TX_BB_IP0
E26	DVSS	W25	DPI_D2	AF14	TX_BB_QP0
J19	DVDD_GPU	W26	DPI_D3	AF15	DVSS
F1	BT_IN	T24	DSI0_D3N	AF16	PRX_BB_I1
F2	BT_IP	T25	DSI0_D3P	AF17	DRX_BB_Q1
F3	DVSS	T26	DSI0_D1N	AF18	AUXIN1
F4	DVSS	T27	DSI0_D0P	AF19	AUXIN0
F5	DVSS	U1	CSI2A_L0N	AF20	RFIC0_BSI_D0
F9	DVSS	U2	CSI2A_L0P	AF21	RFIC0_BSI_CK
F10	DVSS	U3	CSI2A_L2N	AF22	SCL3
F11	DVSS	U4	CSI2A_L2P	AF23	IDDIG
F12	EMI0_DQS1_T	U5	DVSS	AF24	SIM1_SIO
F13	EMI1_DQS1_C	AA10	DVDD_PROC_B	AB27	DVDD28_MSDC1

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
F16	EMI1_CK_C	AB9	DVDD_PROC_B	AF26	DRVBUS
F17	DVSS	AC9	DVDD_PROC_B	AG1	EINT3
F18	DVSS	AC10	DVDD_PROC_B	AG2	EINT2
F19	DVSS	U13	DVSS	AG3	SPI_CSB
F20	EMI1_DQ0	U15	DVDD_CORE	AG4	BPI_PA_VM1
F21	EMI1_DQS0_T	U17	DVSS	AG5	BPI_BUS2
F23	UFS_CKIN_26M	U19	DVDD_CORE	AG6	MISC_BSI_DO_2
J20	DVDD_GPU	U21	DVDD_CORE	AG7	MISC_BSI_DO_1
F25	AVDD33_USB	U23	DVSS	AG8	DVSS
F26	USB_DM	U24	DSI0_CKN	AG9	DVSS
F27	AVDD18_USB	U25	DSI0_CKP	AG11	TX_BB_IP1
G1	BT_QP	U26	DSI0_D1P	AG12	TX_BB_QN1
G2	BT_QN	V1	CSI2B_L0N	AG13	TX_BB_IN0
G3	DVSS	V2	CSI2B_L0P	AG14	TX_BB_QN0
G4	DVSS	V3	CSI2B_L1N	AG15	DVSS
G5	DVSS	V4	CSI2B_L1P	AG16	PRX_BB_Q1
G6	DVSS	V5	DVSS	AG17	DRX_BB_I1
G9	AVDD18_DDR	V8	DVSS	AG18	AUXIN4
G14	AVDDQ_EMI	V9	DVSS	AG19	I2S2_DI
G15	AVDDQ_EMI	V10	DVSS	AG20	RFIC0_BSI_D2
G18	AVDD2_EMI	V12	DVSS	AG21	I2S1_DO
G21	DVSS	V14	DVSS	AG22	SDA3
G23	MSDC0_DAT6	V16	DVDD_CORE	AG23	I2S1_BCK
G24	CHD_DM	V18	DVSS	AG24	INT_SIM1
G25	CHD_DP	V20	DVDD_CORE	AG25	INT_SIM2
G26	USB_DP	AC11	DVDD_PROC_B	AG26	DSI_TE
H2	DVSS	AB26	DPI_D4	AF25	DVDD28_SIM1
H3	CONN_HRST_B	V23	AVDD12_DSI	AH1	KPROW1
H4	CONN_BT_CLK	V24	DSI0_D2N	AH2	SPI_MO
H5	CONN_BT_DATA	V25	DSI0_D2P	AH3	BPI_PA_VM0
H6	CONN_WF_CTRL2	V26	DVSS	AH4	BPI_OLAT0
H8	XIN_WBG	V27	AVDD04_DSI	AH5	BPI_BUS1
H10	AVDDQ_EMI	W1	DVSS	AH6	BPI_BUS7
H11	AVDD2_EMI	W2	SDA4	AH7	MISC_BSI_CK_1
H12	AVDDQ_EMI	W3	AVDD12_CSI	AH8	DVSS
H13	AVDD2_EMI	W4	EINT9	AH9	DVSS
H16	AVDD2_EMI	W5	SRCLKENAI	AH10	DET_QP1
H17	AVDDQ_EMI	W6	CAM_PDN0	AH11	DET_IN1
H19	AVDDQ_EMI	AD9	DVDD_PROC_B	AH12	DET_IP1
H21	DVDD_CORE	AD10	DVDD_PROC_B	AH13	DET_QN0
H22	AVDD12_USB	U7	DVDD_PROC_L	AH14	DET_QP0
H23	AVDD18_SSUSB	W12	DVSS	AH15	DVSS
H24	DVSS	W13	DVSS	AH16	DRX_BB_I0

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
H25	DVSS	W15	DVDD_CORE	AH17	DRX_BB_Q0
H26	DVSS	W17	DVSS	AH18	DVSS
H27	SSUSB_RXP	W19	DVDD_CORE	AH19	AVDD18_MD
J1	GPS_Q	W21	DVSS	AH20	AVDD12_MD
J2	GPS_I	W22	SPI1_MI	AH21	AVDD18_AP
J3	DVSS	AB23	DPI_D5	AH22	BPI_BUS9
J4	CONN_TOP_CLK	W24	DPI_D6	AH23	DISP_PWM
J5	CONN_TOP_DATA	Y24	DPI_D7	AH24	SCL5
J6	CONN_WF_CTRL0	AB24	DPI_D8	AH25	SDA5
J7	CONN_WF_CTRL1	U8	DVDD_PROC_L	AH26	BPI_OLAT1
J8	DVSS	Y2	SCL4	AH27	LCM_RST
J10	DVSS	Y4	EINT10	AJ1	NC_AJ1
J11	DVDD_CORE	Y5	CAM_PDN1	AJ2	SPI_MI
L19	DVDD_GPU	Y26	DPI_D9	AJ4	BPI_ANT1
J13	DVSS	AC26	DPI_DE	AJ5	BPI_BUS6
J14	EMI_TN	Y8	DVSS	AJ7	MISC_BSI_CK_0
J15	EMI_TP	Y9	DVSS	AJ8	MISC_BSI_DO_0
J16	DVDD_CORE	Y10	DVSS	AJ9	DVSS
J17	DVSS	Y12	TN_PLLGP1	AJ10	DET_QN1
M20	DVDD_GPU	Y13	TP_PLLGP1	AJ12	DET_IN0
N19	DVDD_GPU	Y14	DVSS	AJ13	DET_IP0
J22	AUD_DAT_MOSI0	U9	DVDD_PROC_L	AJ15	PRX_BB_Q0
J23	DVSS	Y16	DVDD_CORE	AJ16	PRX_BB_I0
J24	SSUSB_TXN	Y18	DVSS	AJ18	REFP
J25	SSUSB_TXP	Y20	DVDD_CORE	AE27	DVDD28_SIM2
J26	DVSS	Y22	SPI1_MO	AJ22	BPI_BUS10
J27	SSUSB_RXN	Y23	DPI_HSYNC	AJ24	BPI_ANT0
K3	CAM_RST3	AA24	DPI_VSYNC	AJ25	BPI_ANT2
K4	CAM_CLK2	R25	PERIPHERAL_EN0	AJ26	BPI_BUS8
K5	CAM_RST2	L25	PERIPHERAL_EN1	AJ27	NC_AJ27
K6	CONN_WB_PTA	U10	DVDD_PROC_L		

Table 2-2. Pin coordinate LPDDR3

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC_A1	K10	DVSS	AA2	CAM_RST1
A2	EMI_EXTR	K12	DVDD_CORE	AA3	CAM_RST0
A3	EMI0_CA4	K14	DVSS	AA4	CAM_CLK0
A5	EMI0_CA6	K16	DVDD_CORE	AA5	KPROW0
A7	EMI0_CS1	K18	DVSS	AA6	PWM_A
A9	EMI0_DQ19	K22	PERIPHERAL_EN8	AA7	PERIPHERAL_EN14
A11	EMI0_DQ17	K23	SYSRSTB	AA10	DVDD_PROC_B
A13	EMI0_DQ1	K24	DVSS	AA12	DVSS

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A15	EMI0_DQ7	K25	DVSS	AA13	AVDD12_PLLGP
A17	EMI0_DQ14	K26	RTC32K_CK	AA15	DVDD_MODEM
A19	EMI0_DQ31	K27	AVDD09_SSUSB	AA17	DVSS
A21	DVSS	L1	DVSS	AA19	DVDD_MODEM
A22	UFS_RX0_RXP	L2	DVDD18_IORT	AA21	DVSS
A24	UFS_TX0_N	L3	CAM_PDN3	AA22	SPI1_CLK
A26	MSDC0_DAT2	L4	CAM_CLK3	AA23	DPI_D11
A27	NC_A27	L5	CAM_PDN2	AA24	DPI_VSYNC
B1	WF_IP	L9	DVSS	AA25	DPI_D1
B2	AVDD18_WBG	L11	DVDD_CORE	AA26	DPI_D10
B3	EMI0_CA7	L13	DVSS	AA27	DVDD18_MSDC1
B4	NC_B4	L15	DVDD_CORE	AB1	SDA2
B5	EMI0_CA3	L17	DVSS	AB2	SCL2
B6	NC_B6	L19	DVDD_GPU	AB4	EINT1
B7	NC_B7	L22	PERIPHERAL_EN3	AB5	EINT0
B9	DVSS	L23	AUD_DAT_MISO1	AB6	SCL0
B10	EMI0_DQ20	L24	TESTMODE	AB7	DVDD_CORE
B11	EMI0_DQ22	L25	PERIPHERAL_EN1	AB8	DVSS
B13	DVSS	L26	AUD_SYNC_MOSI	AB9	DVDD_PROC_B
B14	EMI0_DQ3	M1	CSI1A_L0N	AB13	AVDD18_PLLGP
B15	EMI0_DMI0	M2	CSI1A_L0P	AB14	DVSS
B17	EMI0_DQ15	M3	CSI1A_L1P	AB16	DVDD_MODEM
B18	EMI0_DMI3	M4	CSI1A_L1N	AB18	DVSS
B19	EMI0_DQ28	M5	DVSS	AB20	DVDD_MODEM
B21	DVSS	M10	DVSS	AB21	DVSS
B22	UFS_RX0_RXN	M12	DVDD_CORE	AB22	DVDD_CORE
B23	DVSS	M14	DVSS	AB23	DPI_D5
B24	UFS_TX0_P	M16	DVDD_CORE	AB24	DPI_D8
B25	DVSS	M18	DVSS	AB25	SPI1_CSB
B26	MSDC0_DAT0	M20	DVDD_GPU	AB26	DPI_D4
B27	MSDC0_DAT1	M22	PERIPHERAL_EN2	AB27	DVDD28_MSDC1
C1	WF_IN	M23	WATCHDOG	AC2	CAM_CLK1
C2	AVDD12_WBG	M24	AUD_CLK_MOSI	AC3	EINT4
C3	DVSS	M25	AUD_CLK_MISO	AC4	KPCOL0
C4	NC_C4	M26	AUD_SYNC_MISO	AC5	SDA0
C5	EMI0_CA2	M27	DVDD18_IOLT	AC6	BPI_BUS0
C6	DVSS	N1	CSI1A_L2P	AC7	AVDD18_CPU
C7	EMI0_CA1	N2	CSI1A_L2N	AC9	DVDD_PROC_B
C8	EMI0_DMI2	N3	CSI1B_L0P	AC10	DVDD_PROC_B
C9	EMI0_DQ16	N4	CSI1B_L0N	AC11	DVDD_PROC_B
C10	DVSS	N5	CSI0A_L2N_T1C	AC12	DVSS
C11	DVSS	N9	DVSS	AC13	DVDD_SRAM_PROC_B
C12	EMI0_DQ0	N11	DVDD_CORE	AC14	DVDD_SRAM_CORE

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C13	EMI0_DQ2	N13	DVSS	AC15	DVDD_MODEM
C14	EMI0_DQ4	N15	DVDD_CORE	AC17	DVSS
C15	EMI0_DQ8	N17	DVSS	AC19	DVDD_MODEM
C16	NC_C16	N19	DVDD_GPU	AC22	DVDD_CORE
C17	EMI0_DQ9	N21	DVSS	AC23	MSDC1_DAT2
C18	DVSS	N22	PERIPHERAL_EN6	AC24	MSDC1_CLK
C19	DVSS	N23	PWRAP_SPI0_CSN	AC25	DPI_CK
C20	EMI0_DQ30	N24	AUD_DAT_MISO0	AC26	DPI_DE
C21	EMI0_DQ29	N25	SCP_VREQ_VAO	AD1	UTXD0
C22	AVDD09_UFS	N26	SCL6	AD2	URXD0
C23	AVDD12_UFS	N27	AUD_DAT_MOSI1	AD4	EINT8
C24	DVSS	P1	CSI1B_L1N	AD5	BPI_BUS5
C25	MSDC0_DAT5	P2	CSI1B_L1P	AD6	MISC_BSI_CK_3
C26	MSDC0_DAT4	P3	CSI0A_L0N_T0B	AD7	DVDD_CORE
C27	MSDC0_CMD	P4	CSI0A_L0P_T0A	AD8	DVSS
D1	WF_QP	P5	CSI0A_L2P_T1B	AD9	DVDD_PROC_B
D2	WF_QN	P7	DVDD_CORE	AD10	DVDD_PROC_B
D3	DVSS	P10	DVSS	AD16	DVDD_MODEM
D4	NC_D4	P12	DVDD_CORE	AD19	PERIPHERAL_EN13
D5	NC_D5	P14	DVSS	AD20	I2S1_MCK
D6	EMI0_CA5	P16	DVDD_CORE	AD21	I2S1_LRCK
D7	EMI0_CKE1	P18	DVSS	AD22	PERIPHERAL_EN12
D8	EMI0_CS0	P20	DVDD_GPU	AD23	SIM2_SCLK
D9	EMI0_DQ18	P21	DVDD_CORE	AD24	MSDC1_DAT0
D10	EMI0_CK_T	P22	ANT_SEL0	AD25	PERIPHERAL_EN5
D11	EMI0_DQ21	P23	PWRAP_SPI0_CK	AD26	MSDC1_CMD
D12	DVSS	P24	PWRAP_SPI0_MI	AD27	MSDC1_DAT3
D14	EMI0_DQ5	P25	PWRAP_SPI0_MO	AE1	EINT7
D15	EMI0_DQ6	P26	SDA6	AE2	EINT6
D16	DVSS	R1	CSI0A_L1N_T1A	AE3	KPCOL1
D17	EMI0_DQ11	R2	CSI0A_L1P_T0C	AE4	SCL1
D18	EMI0_DQ10	R3	CSI0B_L0P_T0A	AE5	BPI_BUS4
D19	EMI0_DQ13	R4	CSI0B_L0N_T0B	AE6	MISC_BSI_DO_3
D20	EMI0_DQ24	R5	CSI2A_L1N	AE7	CDM5P5A
D21	DVSS	R7	DVDD_CORE	AE10	DVSS
D22	EMI_RESET_N	R8	DVDD_CORE	AE11	RFIC_ET0_P
D23	AVDD18_UFS	R9	DVSS	AE12	RFIC_ET0_N
D24	MSDC0_CLK	R11	DVDD_CORE	AE13	APC
D25	MSDC0_RSTB	R13	DVSS	AE14	DVSS
D26	MSDC0_DAT7	R15	DVDD_CORE	AE15	DVSS
E2	DVSS	R17	DVSS	AE16	DVSS
E3	DVSS	R19	DVDD_GPU	AE17	MAIN_X26M_IN
E4	DVSS	R22	ANT_SEL2	AE18	AUXIN3

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
E5	EMI0_CA9	R23	SRCLKENA0	AE19	AUXIN2
E6	EMI0_CA8	R24	SRCLKENA1	AE20	RFIC0_BSI_D1
E7	NC_E7	R25	PERIPHERAL_EN0	AE21	RFIC0_BSI_EN
E8	EMI0_CKE0	R26	DVSS	AE22	SIM1_SRST
E9	EMI0_CA0	R27	DSI0_D0N	AE23	SIM1_SCLK
E10	EMI0_CK_C	T1	CSI0B_L1N_T1A	AE24	SIM2_SIO
E11	EMI0_DQ23	T2	CSI0B_L1P_T0C	AE25	SIM2_SRST
E12	EMI0_DQS2_C	T3	CSI0B_L2P_T1B	AE26	MSDC1_DAT1
E13	EMI0_DQS0_T	T4	CSI0B_L2N_T1C	AE27	DVDD28_SIM2
E14	DVSS	T5	CSI2A_L1P	AF2	EINT5
E15	DVSS	T7	DVDD_CORE	AF3	SPI_CLK
E16	EMI0_DQS1_T	T8	DVDD_CORE	AF4	SDA1
E17	EMI0_DMI1	T10	DVSS	AF5	BPI_BUS3
E18	EMI0_DQ12	T11	DVDD_SRAM_CORE	AF6	MISC_BSI_CK_2
E19	EMI0_DQ25	T12	DVDD_CORE	AF7	CDM3P5A
E20	EMI0_DQ27	T14	DVSS	AF8	DVSS
E21	EMI0_DQS3_C	T16	DVDD_CORE	AF9	DVSS
E22	UFS_RST_N	T18	DVDD_SRAM_GPU	AF11	TX_BB_IN1
E24	MSDC0_DAT3	T20	DVDD_GPU	AF12	TX_BB_QP1
E25	MSDC0_DSL	T21	DVSS	AF13	TX_BB_IP0
E26	DVSS	T22	PERIPHERAL_EN7	AF14	TX_BB_QP0
E27	DVDD18_MSDC0	T23	ANT_SEL1	AF15	DVSS
F1	BT_IN	T24	DSI0_D3N	AF16	PRX_BB_I1
F2	BT_IP	T25	DSI0_D3P	AF17	DRX_BB_Q1
F3	DVSS	T26	DSI0_D1N	AF18	AUXIN1
F4	DVSS	T27	DSI0_D0P	AF19	AUXIN0
F5	DVSS	U1	CSI2A_L0N	AF20	RFIC0_BSI_D0
F9	DVSS	U2	CSI2A_L0P	AF21	RFIC0_BSI_CK
F10	DVSS	U3	CSI2A_L2N	AF22	SCL3
F11	DVSS	U4	CSI2A_L2P	AF23	IDDIG
F12	EMI0_DQS2_T	U5	DVSS	AF24	SIM1_SIO
F13	EMI0_DQS0_C	U7	DVDD_PROC_L	AF25	DVDD28_SIM1
F16	EMI0_DQS1_C	U8	DVDD_PROC_L	AF26	DRVBUS
F17	DVSS	U9	DVDD_PROC_L	AG1	EINT3
F18	DVSS	U10	DVDD_PROC_L	AG2	EINT2
F19	DVSS	U13	DVSS	AG3	SPI_CSB
F20	EMI0_DQ26	U15	DVDD_CORE	AG4	BPI_PA_VM1
F21	EMI0_DQS3_T	U17	DVSS	AG5	BPI_BUS2
F23	UFS_CKIN_26M	U19	DVDD_CORE	AG6	MISC_BSI_DO_2
F24	DVDD_VQPS	U21	DVDD_CORE	AG7	MISC_BSI_DO_1
F25	AVDD33_USB	U23	DVSS	AG8	DVSS
F26	USB_DM	U24	DSI0_CKN	AG9	DVSS
F27	AVDD18_USB	U25	DSI0_CKP	AG11	TX_BB_IP1

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
G1	BT_QP	U26	DSI0_D1P	AG12	TX_BB_QN1
G2	BT_QN	V1	CSI2B_L0N	AG13	TX_BB_IN0
G3	DVSS	V2	CSI2B_L0P	AG14	TX_BB_QN0
G4	DVSS	V3	CSI2B_L1N	AG15	DVSS
G5	DVSS	V4	CSI2B_L1P	AG16	PRX_BB_Q1
G6	DVSS	V5	DVSS	AG17	DRX_BB_I1
G9	AVDD18_DDR	V8	DVSS	AG18	AUXIN4
G14	AVDDQ_EMI	V9	DVSS	AG19	I2S2_DI
G15	AVDDQ_EMI	V10	DVSS	AG20	RFIC0_BSI_D2
G18	AVDD2_EMI	V12	DVSS	AG21	I2S1_DO
G21	DVSS	V14	DVSS	AG22	SDA3
G23	MSDC0_DAT6	V16	DVDD_CORE	AG23	I2S1_BCK
G24	CHD_DM	V18	DVSS	AG24	INT_SIM1
G25	CHD_DP	V20	DVDD_CORE	AG25	INT_SIM2
G26	USB_DP	V21	DVDD_SRAM_CORE	AG26	DSI_TE
H2	DVSS	V22	PERIPHERAL_EN9	AG27	DVDD18_SIM
H3	CONN_HRST_B	V23	AVDD12_DSI	AH1	KPROW1
H4	CONN_BT_CLK	V24	DSI0_D2N	AH2	SPI_MO
H5	CONN_BT_DATA	V25	DSI0_D2P	AH3	BPI_PA_VM0
H6	CONN_WF_CTRL2	V26	DVSS	AH4	BPI_OLAT0
H8	XIN_WBG	V27	AVDD04_DSI	AH5	BPI_BUS1
H10	AVDDQ_EMI	W1	DVSS	AH6	BPI_BUS7
H11	AVDD2_EMI	W2	SDA4	AH7	MISC_BSI_CK_1
H12	AVDDQ_EMI	W3	AVDD12_CSI	AH8	DVSS
H13	AVDD2_EMI	W4	EINT9	AH9	DVSS
H16	AVDD2_EMI	W5	SRCLKENAI	AH10	DET_QP1
H17	AVDDQ_EMI	W6	CAM_PDN0	AH11	DET_IN1
H19	AVDDQ_EMI	W7	DVDD_SRAM_PROC_L	AH12	DET_IP1
H21	DVDD_CORE	W9	DVDD_PROC_L	AH13	DET_QN0
H22	AVDD12_USB	W11	DVDD_PROC_L	AH14	DET_QP0
H23	AVDD18_SSUSB	W12	DVSS	AH15	DVSS
H24	DVSS	W13	DVSS	AH16	DRX_BB_I0
H25	DVSS	W15	DVDD_CORE	AH17	DRX_BB_Q0
H26	DVSS	W17	DVSS	AH18	DVSS
H27	SSUSB_RXP	W19	DVDD_CORE	AH19	AVDD18_MD
J1	GPS_Q	W21	DVSS	AH20	AVDD12_MD
J2	GPS_I	W22	SPI1_MI	AH21	AVDD18_AP
J3	DVSS	W23	DPI_D0	AH22	BPI_BUS9
J4	CONN_TOP_CLK	W24	DPI_D6	AH23	DISP_PWM
J5	CONN_TOP_DATA	W25	DPI_D2	AH24	SCL5
J6	CONN_WF_CTRL0	W26	DPI_D3	AH25	SDA5
J7	CONN_WF_CTRL1	W27	DVDD18_IOLM	AH26	BPI_OLAT1
J8	DVSS	Y2	SCL4	AH27	LCM_RST

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Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
J10	DVSS	Y4	EINT10	AJ1	NC_AJ1
J11	DVDD_CORE	Y5	CAM_PDN1	AJ2	SPI_MI
J12	DVDD_SRAM_CORE	Y6	PERIPHERAL_EN11	AJ4	BPI_ANT1
J13	DVSS	Y7	PERIPHERAL_EN10	AJ5	BPI_BUS6
J14	NC_J14	Y8	DVSS	AJ7	MISC_BSI_CK_0
J15	EVREF	Y9	DVSS	AJ8	MISC_BSI_DO_0
J16	DVDD_CORE	Y10	DVSS	AJ9	DVSS
J17	DVSS	Y12	TN_PLLGP1	AJ10	DET_QN1
J19	DVDD_GPU	Y13	TP_PLLGP1	AJ12	DET_IN0
J20	DVDD_GPU	Y14	DVSS	AJ13	DET_IP0
J22	AUD_DAT_MOSI0	Y15	DVDD_SRAM_CORE	AJ15	PRX_BB_Q0
J23	DVSS	Y16	DVDD_CORE	AJ16	PRX_BB_I0
J24	SSUSB_TXN	Y18	DVSS	AJ18	REFP
J25	SSUSB_TXP	Y20	DVDD_CORE	AJ21	DVDD18_IOBL
J26	DVSS	Y22	SPI1_MO	AJ22	BPI_BUS10
J27	SSUSB_RXN	Y23	DPI_HSYNC	AJ24	BPI_ANT0
K3	CAM_RST3	Y24	DPI_D7	AJ25	BPI_ANT2
K4	CAM_CLK2	Y25	PERIPHERAL_EN4	AJ26	BPI_BUS8
K5	CAM_RST2	Y26	DPI_D9	AJ27	NC_AJ27
K6	CONN_WB_PTA	AA1	DVDD18_IORB		

2.1.3 Detailed Pin Description

Table 2-3. Acronym for pin type

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-4. Detailed pin description

Pin name	Pin no.	Type	Description	Power domain
System				
SYSRSTB	K23	DI	System reset input	DVDD18
WATCHDOG	M23	DIO	Watchdog reset output	DVDD18
TESTMODE	L24	DI	Test mode	DVDD18
RTC32K_CK	K26	DIO	RTC 32K input	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
SRCLKENA0	R23	DIO	Output signal; control 26Hz/Buck/LDO normal mode or sleep mode. (High: normal mode; low: sleep mode or low power mode)	DVDD18
SRCLKENA1	R24	DIO	Output signal; control VRF18. (High: VRF18 on, Low: VRF18 off)	DVDD18
SRCLKENAI	W5	DIO	Input signal; NFC 26MHz request signal. (High: NFC chip requests system to provide 26MHz to NFC chip)	DVDD18
EINT0	AB5	DIO	External interrupt input	DVDD18
EINT1	AB4	DIO	External interrupt input	DVDD18
EINT2	AG2	DIO	External interrupt input	DVDD18
EINT3	AG1	DIO	External interrupt input	DVDD18
EINT4	AC3	DIO	External interrupt input	DVDD18
EINT5	AF2	DIO	External interrupt input	DVDD18
EINT6	AE2	DIO	External interrupt input	DVDD18
EINT7	AE1	DIO	External interrupt input	DVDD18
EINT8	AD4	DIO	External interrupt input	DVDD18
EINT9	W4	DIO	External interrupt input	DVDD18
EINT10	Y4	DIO	External interrupt input	DVDD18
PMIC				
PWRAP_SPI0_MO	P25	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_MI	P24	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CSN	N23	DIO	PMIC SPI control interface	DVDD18
PWRAP_SPI0_CK	P23	DIO	PMIC SPI control interface	DVDD18
AUD_CLK_MOSI	M24	DIO	PMIC audio input interface	DVDD18
AUD_CLK_MISO	M25	DIO	PMIC audio input interface	DVDD18
AUD_SYNC_MOSI	L26	DIO	PMIC audio input interface	DVDD18
AUD_SYNC_MISO	M26	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MISO0	N24	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MISO1	L23	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI0	J22	DIO	PMIC audio input interface	DVDD18
AUD_DAT_MOSI1	N27	DIO	PMIC audio input interface	DVDD18
SCP_VREQ_VAO	N25	DIO	SCP to PMIC normal voltage request	DVDD18
SIM				
SIM1_SCLK	AE23	DIO	SIM1 clock, PMIC interface	DVDD28_SIM1
SIM1_SIO	AF24	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM1_SRST	AE22	DIO	SIM1 data, PMIC interface	DVDD28_SIM1
SIM2_SCLK	AD23	DIO	SIM2 clock, PMIC interface	DVDD28_SIM2
SIM2_SIO	AE24	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
SIM2_SRST	AE25	DIO	SIM2 data, PMIC interface	DVDD28_SIM2
INT_SIM1	AG24	DIO	SIM1 interrupt	DVDD18
INT_SIM2	AG25	DIO	SIM2 interrupt	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
I2S				
I2S1_BCK	AG23	DIO	I2S interface	DVDD18
I2S2_DI	AG19	DIO	I2S interface	DVDD18
I2S1_DO	AG21	DIO	I2S interface	DVDD18
I2S1_LRCK	AD21	DIO	I2S interface	DVDD18
I2S1_MCK	AD20	DIO	I2S interface	DVDD18
LCD				
DSI_TE	AG26	DIO	Parallel display interface tearing effect	DVDD18
LCM_RST	AH27	DIO	Parallel display interface reset signal	DVDD18
DPI_HSYNC	Y23	DIO	Parallel display interface HSYNC	DVDD18
DPI_VSYNC	AA24	DIO	Parallel display interface VSYNC	DVDD18
DPI_CK	AC25	DIO	Parallel display interface CLK	DVDD18
DPI_DE	AC26	DIO	Parallel display interface DE	DVDD18
DPI_D11	AA23	DIO	Data pin 11 for DPI parallel LCD interface	DVDD18
DPI_D10	AA26	DIO	Data pin 10 for DPI parallel LCD interface	DVDD18
DPI_D9	Y26	DIO	Data pin 9 for DPI parallel LCD interface	DVDD18
DPI_D8	AB24	DIO	Data pin 8 for DPI parallel LCD interface	DVDD18
DPI_D7	Y24	DIO	Data pin 7 for DPI parallel LCD interface	DVDD18
DPI_D6	W24	DIO	Data pin 6 for DPI parallel LCD interface	DVDD18
DPI_D5	AB23	DIO	Data pin 5 for DPI parallel LCD interface	DVDD18
DPI_D4	AB26	DIO	Data pin 4 for DPI parallel LCD interface	DVDD18
DPI_D3	W26	DIO	Data pin 3 for DPI parallel LCD interface	DVDD18
DPI_D2	W25	DIO	Data pin 2 for DPI parallel LCD interface	DVDD18
DPI_D1	AA25	DIO	Data pin 1 for DPI parallel LCD interface	DVDD18
DPI_D0	W23	DIO	Data pin 0 for DPI parallel LCD interface	DVDD18
PWM				
DISP_PWM	AH23	DIO	Display PWM output	DVDD18
PWM_A	AA6	DIO	PWM_A	DVDD18
Keypad interface				
KPCOL0	AC4	DIO	Keypad column 0	DVDD18
KPCOL1	AE3	DIO	Keypad column 1	DVDD18
KPROW0	AA5	DIO	Keypad row 0	DVDD18
KPROW1	AH1	DIO	Keypad row 1	DVDD18
SPI				
SPI_CSB	AG3	DIO	SPI chip select	DVDD18
SPI_MI	AJ2	DIO	SPI data in	DVDD18
SPI_MO	AH2	DIO	SPI data out	DVDD18
SPI_CLK	AF3	DIO	SPI clock	DVDD18
SPI1_CSB	AB25	DIO	SPI1 chip select	DVDD18
SPI1_MI	W22	DIO	SPI1 data in	DVDD18
SPI1_MO	Y22	DIO	SPI1 data out	DVDD18
SPI1_CLK	AA22	DIO	SPI1 clock	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
UR				
UTXD0	AD1	DIO	UR0 interdace	DVDD18
URXD0	AD2	DIO	SPI0 data in	DVDD18
RF interface				
BPI_BUS0	AC6	DIO	BPI_BUS0	DVDD18
BPI_BUS1	AH5	DIO	BPI_BUS1	DVDD18
BPI_BUS2	AG5	DIO	BPI_BUS2	DVDD18
BPI_BUS3	AF5	DIO	BPI_BUS3	DVDD18
BPI_BUS4	AE5	DIO	BPI_BUS4	DVDD18
BPI_BUS5	AD5	DIO	BPI_BUS5	DVDD18
BPI_BUS6	AJ5	DIO	BPI_BUS6	DVDD18
BPI_BUS7	AH6	DIO	BPI_BUS7	DVDD18
BPI_BUS8	AJ26	DIO	BPI_BUS8	DVDD18
BPI_BUS9	AH22	DIO	BPI_BUS9	DVDD18
BPI_BUS10	AJ22	DIO	BPI_BUS10	DVDD18
BPI_ANT0	AJ24	DIO	BPI_ANT0	DVDD18
BPI_ANT1	AJ4	DIO	BPI_ANT1	DVDD18
BPI_ANT2	AJ25	DIO	BPI_ANT2	DVDD18
BPI_PA_VM0	AH3	DIO	BPI_PA_VM0	DVDD18
BPI_PA_VM1	AG4	DIO	BPI_PA_VM1	DVDD18
BPI_OLAT0	AH4	DIO	BPI Control	DVDD18
BPI_OLAT1	AH26	DIO	BPI Control	DVDD18
ANT_SEL0	P22	DIO	BPI Control	DVDD18
ANT_SEL1	T23	DIO	BPI Control	DVDD18
ANT_SEL2	R22	DIO	BPI Control	DVDD18
MISC_BSI_DO_0	AJ8	DIO	MISC_BSI_DO_0	DVDD18
MISC_BSI_CK_0	AJ7	DIO	MISC_BSI_CK_0	DVDD18
MISC_BSI_DO_1	AG7	DIO	MISC_BSI_DO_1	DVDD18
MISC_BSI_CK_1	AH7	DIO	MISC_BSI_CK_1	DVDD18
MISC_BSI_DO_2	AG6	DIO	MISC_BSI_DO_2	DVDD18
MISC_BSI_CK_2	AF6	DIO	MISC_BSI_CK_2	DVDD18
MISC_BSI_DO_3	AE6	DIO	MISC_BSI_DO_3	DVDD18
MISC_BSI_CK_3	AD6	DIO	MISC_BSI_CK_3	DVDD18
BSI				
RFIC0_BSI_CK	AF21	DIO	RFIC0 BSI CLK	DVDD18
RFIC0_BSI_D0	AF20	DIO	RFIC0 BSI DATA0	DVDD18
RFIC0_BSI_D1	AE20	DIO	RFIC0 BSI DATA1	DVDD18
RFIC0_BSI_D2	AG20	DIO	RFIC0 BSI DATA2	DVDD18
RFIC0_BSI_EN	AE21	DIO	RFIC0 BSI CS	DVDD18
MSDC0				
MSDC0_CLK	D24	DIO	MSDC0 clock output	DVDD18_MSDC0
MSDC0_CMD	C27	DIO	MSDC0 command pin	DVDD18_MSDC0

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Pin name	Pin no.	Type	Description	Power domain
MSDC0_DAT0	B26	DIO	MSDC0 data0 pin	DVDD18_MSDC0
MSDC0_DAT1	B27	DIO	MSDC0 data1 pin	DVDD18_MSDC0
MSDC0_DAT2	A26	DIO	MSDC0 data2 pin	DVDD18_MSDC0
MSDC0_DAT3	E24	DIO	MSDC0 data3 pin	DVDD18_MSDC0
MSDC0_DAT4	C26	DIO	MSDC0 data4 pin	DVDD18_MSDC0
MSDC0_DAT5	C25	DIO	MSDC0 data5 pin	DVDD18_MSDC0
MSDC0_DAT6	G23	DIO	MSDC0 data6 pin	DVDD18_MSDC0
MSDC0_DAT7	D26	DIO	MSDC0 data7 pin	DVDD18_MSDC0
MSDC0_DSL	E25	DIO	MSDC0 DSL pin	DVDD18_MSDC0
MSDC0_RSTB	D25	DIO	MSDC0 reset pin	DVDD18_MSDC0
MSDC1				
MSDC1_CLK	AC24	DIO	MSDC1 clock output	DVDD28_MSDC1
MSDC1_CMD	AD26	DIO	MSDC1 command pin	DVDD28_MSDC1
MSDC1_DAT0	AD24	DIO	MSDC1 data0 pin	DVDD28_MSDC1
MSDC1_DAT1	AE26	DIO	MSDC1 data1 pin	DVDD28_MSDC1
MSDC1_DAT2	AC23	DIO	MSDC1 data2 pin	DVDD28_MSDC1
MSDC1_DAT3	AD27	DIO	MSDC1 data3 pin	DVDD28_MSDC1
EFUSE				
DVDD_VQPS	F24	DIO	E-FUSE blowing power control	DVDD_VQPS
EMI				
EMI0_DQ0 (EMI0_CA9)	E5	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ1 (NC)	D5	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ2 (EMI0_CA8)	E6	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ3 (EMI0_CA5)	D6	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ4 (EMI0_CA7)	B3	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ5 (EMI0_CA2)	C5	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ6 (EMI0_CA6)	A5	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ7 (EMI0_CA4)	A3	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ8 (EMI0_DQ22)	B11	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ9 (EMI0_DQ23)	E11	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ10 (EMI0_DQ20)	B10	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ11 (EMI0_DQ19)	A9	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ12 (EMI0_DQ17)	A11	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ13 (EMI0_DQ18)	D9	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ14 (EMI0_DQ16)	C9	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQ15 (EMI0_DQ21)	D11	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI

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Pin name	Pin no.	Type	Description	Power domain
EMI0_DQS0_C (NC)	C4	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQS0_T (NC)	D4	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQS1_C (EMI0_DQS2_C)	E12	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DQS1_T (EMI0_DQS2_T)	F12	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_CA0	E9	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA1	C7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CA2 (EMI0_CA3)	B5	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_CA3 (NC)	B6	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_CA4 (NC)	B7	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_CA5 (NC)	E7	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_CS0	D8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CS1	A7	DIO	DRAM interface	AVDDQ_EMI
EMI0_DMI0 (NC)	B4	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_DMI1 (EMI0_DMI2)	C8	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI0_CKE0	E8	DIO	DRAM interface	AVDDQ_EMI
EMI0_CKE1	D7	DIO	DRAM interface	AVDDQ_EMI
EMI0_CK_C	E10	DIO	DRAM interface	AVDDQ_EMI
EMI0_CK_T	D10	DIO	DRAM interface	AVDDQ_EMI
EMI1_DQ0 (EMI0_DQ26)	F20	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ1 (EMI0_DQ27)	E20	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ2 (EMI0_DQ24)	D20	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ3 (EMI0_DQ25)	E19	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ4 (EMI0_DQ30)	C20	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ5 (EMI0_DQ28)	B19	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ6 (EMI0_DQ31)	A19	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ7 (EMI0_DQ29)	C21	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ8 (EMI0_DQ2)	C13	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ9 (EMI0_DQ4)	C14	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ10 (EMI0_DQ1)	A13	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ11 (EMI0_DQ6)	D15	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ12 (EMI0_DQ0)	C12	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ13 (EMI0_DQ7)	A15	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ14 (EMI0_DQ3)	B14	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQ15 (EMI0_DQ5)	D14	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQS0_C (EMI0_DQS3_C)	E21	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQS0_T (EMI0_DQS3_T)	F21	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DQS1_C (EMI0_DQS0_C)	F13	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI

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Pin name	Pin no.	Type	Description	Power domain
EMI1_DQS1_T (EMI0_DQS0_T)	E13	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CA0 (EMI0_DQ11)	D17	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CA1 (EMI0_DQ8)	C15	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CA2 (EMI0_DQ15)	B17	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CA3 (EMI0_DQ14)	A17	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CA4 (EMI0_DQ9)	C17	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CA5 (EMI0_DQ13)	D19	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CS0 (EMI0_DMI1)	E17	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CS1 (NC)	C16	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DMI0 (EMI0_DMI3)	B18	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_DMI1 (EMI0_DMI0)	B15	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CKE0 (EMI0_DQ10)	D18	DIO	DRAM interface LP4 (LP3)	AVDD2_EMI
EMI1_CKE1 (EMI0_DQ12)	E18	DIO	DRAM interface LP4 (LP3)	AVDD2_EMI
EMI1_CK_C (EMI0_DQS1_C)	F16	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI1_CK_T (EMI0_DQS1_T)	E16	DIO	DRAM interface LP4 (LP3)	AVDDQ_EMI
EMI_EXTR	A2	DIO	DRAM interface	AVDD2_EMI
EMI_RESET_N	D22	DIO	DRAM interface	AVDD2_EMI
EMI_TP (EVREF)	J15	DIO	DRAM interface LP4 (LP3)	AVDD2_EMI
EMI_TN (NC)	J14	DIO	DRAM interface LP4 (LP3)	AVDD18_DDR
AVDD18_DDR	G9	P	DRAM power	AVDD18_DDR
AVDD2_EMI	G18	P	DRAM power	AVDD2_EMI
AVDD2_EMI	G18	P	DRAM power	AVDD2_EMI
AVDD2_EMI	G18	P	DRAM power	AVDD2_EMI
AVDD2_EMI	G18	P	DRAM power	AVDD2_EMI
CAM				
CAM_CLK0	AA4	DIO	Master clock to 1st sensor	DVDD18
CAM_CLK1	AC2	DIO	Master clock to 2nd sensor	DVDD18
CAM_CLK2	K4	DIO	Master clock to 3rd sensor	DVDD18
CAM_CLK3	L4	DIO	Master clock to 4th sensor	DVDD18
CAM_RST0	AA3	DIO	Reset control to 1st sensor	DVDD18
CAM_PDN0	W6	DIO	Power down to 1st sensor	DVDD18
CAM_RST1	AA2	DIO	Reset control to 2nd sensor	DVDD18
CAM_PDN1	Y5	DIO	Power down to 2nd sensor	DVDD18
CAM_RST2	K5	DIO	Reset control to 3rd sensor	DVDD18
CAM_PDN2	L5	DIO	Power down to 3rd sensor	DVDD18
CAM_RST3	K3	DIO	Reset control to 4th sensor	DVDD18
CAM_PDN3	L3	DIO	Power down to 4th sensor	DVDD18

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Pin name	Pin no.	Type	Description	Power domain
I2C				
SCL0	AB6	DIO	I2C0 clock	DVDD18
SCL1	AE4	DIO	I2C1 clock	DVDD18
SCL2	AB2	DIO	I2C2 clock	DVDD18
SCL3	AF22	DIO	I2C3 clock	DVDD18
SCL4	Y2	DIO	I2C4 clock	DVDD18
SCL5	AH24	DIO	I2C5 clock	DVDD18
SCL6	N26	DIO	I2C6 clock	DVDD18
SDA0	AC5	DIO	I2C0 data	DVDD18
SDA1	AF4	DIO	I2C1 data	DVDD18
SDA2	AB1	DIO	I2C2 data	DVDD18
SDA3	AG22	DIO	I2C3 data	DVDD18
SDA4	W2	DIO	I2C4 data	DVDD18
SDA5	AH25	DIO	I2C5 data	DVDD18
SDA6	P26	DIO	I2C6 data	DVDD18
CONN				
CONN_BT_CLK	H4	DIO	Connsys BT 2-wire interface	DVDD18
CONN_BT_DATA	H5	DIO	Connsys BT 2-wire interface	DVDD18
CONN_HRST_B	H3	DIO	Connsys reset	DVDD18
CONN_TOP_CLK	J4	DIO	Connsys TOP 2-wire interface	DVDD18
CONN_TOP_DATA	J5	DIO	Connsys TOP 2-wire interface	DVDD18
CONN_WB_PTA	K6	DIO	Connsys WIFI/BT PTA	DVDD18
CONN_WF_CTRL0	J6	DIO	Connsys WIFI 3-wire interface	DVDD18
CONN_WF_CTRL1	J7	DIO	Connsys WIFI 3-wire interface	DVDD18
CONN_WF_CTRL2	H6	DIO	Connsys WIFI 3-wire interface	DVDD18
ABB				
REFP	AJ18	AIO	ABB interface	AVDD18_MD
AUXIN0	AF19	AIO	AuxADC external input channel 0	AVDD18_MD
AUXIN1	AF18	AIO	AuxADC external input channel 1	AVDD18_MD
AUXIN2	AE19	AIO	AuxADC external input channel 2	AVDD18_MD
AUXIN3	AE18	AIO	AuxADC external input channel 3	AVDD18_MD
AUXIN4	AG18	AIO	AuxADC external input channel 4	AVDD18_MD
DET_IN0	AJ12	AIO	RF0 IN detection path	AVDD18_MD
DET_IP0	AJ13	AIO	RF0 IP detection path	AVDD18_MD
DET_QP0	AH14	AIO	RF0 QP detection path	AVDD18_MD
DET_QN0	AH13	AIO	RF0 QN detection path	AVDD18_MD
DET_IN1	AH11	AIO	RF1 IN detection path	AVDD18_MD
DET_IP1	AH12	AIO	RF1 IP detection path	AVDD18_MD
DET_QP1	AH10	AIO	RF1 QP detection path	AVDD18_MD
DET_QN1	AJ10	AIO	RF1 QN detection path	AVDD18_MD
TX_BB_QP0	AF14	AIO	Uplink QP for path0	AVDD18_MD
TX_BB_QN0	AG14	AIO	Uplink QN for path0	AVDD18_MD

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Pin name	Pin no.	Type	Description	Power domain
TX_BB_IN0	AG13	AIO	Uplink IN for path0	AVDD18_MD
TX_BB_IP0	AF13	AIO	Uplink IP for path0	AVDD18_MD
TX_BB_QP1	AF12	AIO	Uplink QP for path1	AVDD18_MD
TX_BB_QN1	AG12	AIO	Uplink QN for path1	AVDD18_MD
TX_BB_IN1	AF11	AIO	Uplink IN for path1	AVDD18_MD
TX_BB_IP1	AG11	AIO	Uplink IP for path1	AVDD18_MD
MAIN_X26M_IN	AE17	AIO	26MHz clock input for AP & 1st modem	AVDD18_MD
PRX_BB_Q0	AJ15	AIO	Main downlink Q-ch for path 0	AVDD18_MD
PRX_BB_I0	AJ16	AIO	Main downlink I-ch for path 0	AVDD18_MD
DRX_BB_Q0	AH17	AIO	Diverse downlink Q-ch for path 0	AVDD18_MD
DRX_BB_I0	AH16	AIO	Diverse downlink I-ch for path 0	AVDD18_MD
PRX_BB_Q1	AG16	AIO	Main downlink Q-ch for path 1	AVDD18_MD
PRX_BB_I1	AF16	AIO	Main downlink I-ch for path 1	AVDD18_MD
DRX_BB_Q1	AF17	AIO	Diverse downlink Q-ch for path 1	AVDD18_MD
DRX_BB_I1	AG17	AIO	Diverse downlink I-ch for path 1	AVDD18_MD
RFIC_ET0_N	AE12	AIO	Envelop tracking DAC0 output P	AVDD18_MD
RFIC_ET0_P	AE11	AIO	Envelop tracking DAC0 output N	AVDD18_MD
APC	AE13	AIO	Automatic power control	AVDD18_MD
MIPI				
DSI0_CKN	U24	AIO	DSI interface	AVDD12_DSI
DSI0_CKP	U25	AIO	DSI interface	AVDD12_DSI
DSI0_D0N	R27	AIO	DSI interface	AVDD12_DSI
DSI0_D0P	T27	AIO	DSI interface	AVDD12_DSI
DSI0_D1N	T26	AIO	DSI interface	AVDD12_DSI
DSI0_D1P	U26	AIO	DSI interface	AVDD12_DSI
DSI0_D2N	V24	AIO	DSI interface	AVDD12_DSI
DSI0_D2P	V25	AIO	DSI interface	AVDD12_DSI
DSI0_D3N	T24	AIO	DSI interface	AVDD12_DSI
DSI0_D3P	T25	AIO	DSI interface	AVDD12_DSI
CSI0A_L0P_T0A	P4	AO	CSI interface	AVDD12_CSI
CSI0A_L0N_T0B	P3	AIO	CSI interface	AVDD12_CSI
CSI0A_L1P_T0C	R2	AIO	CSI interface	AVDD12_CSI
CSI0A_L1N_T1A	R1	AIO	CSI interface	AVDD12_CSI
CSI0A_L2P_T1B	P5	AIO	CSI interface	AVDD12_CSI
CSI0A_L2N_T1C	N5	AIO	CSI interface	AVDD12_CSI
CSI0B_L0P_T0A	R3	AIO	CSI interface	AVDD12_CSI
CSI0B_L0N_T0B	R4	AIO	CSI interface	AVDD12_CSI
CSI0B_L1P_T0C	T2	AIO	CSI interface	AVDD12_CSI
CSI0B_L1N_T1A	T1	AIO	CSI interface	AVDD12_CSI
CSI0B_L2P_T1B	T3	AIO	CSI interface	AVDD12_CSI
CSI0B_L2N_T1C	T4	AIO	CSI interface	AVDD12_CSI
CSI1A_L0P	M2	AIO	CSI interface	AVDD12_CSI

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Pin name	Pin no.	Type	Description	Power domain
CSI1A_L0N	M1	AIO	CSI interface	AVDD12_CSI
CSI1A_L1P	M3	AIO	CSI interface	AVDD12_CSI
CSI1A_L1N	M4	AIO	CSI interface	AVDD12_CSI
CSI1A_L2P	N1	AIO	CSI interface	AVDD12_CSI
CSI1A_L2N	N2	AIO	CSI interface	AVDD12_CSI
CSI1B_L0P	N3	AIO	CSI interface	AVDD12_CSI
CSI1B_L0N	N4	AIO	CSI interface	AVDD12_CSI
CSI1B_L1P	P2	AIO	CSI interface	AVDD12_CSI
CSI1B_L1N	P1	AIO	CSI interface	AVDD12_CSI
CSI2A_L0P	U2	AIO	CSI interface	AVDD12_CSI
CSI2A_L0N	U1	AIO	CSI interface	AVDD12_CSI
CSI2A_L1P	T5	AIO	CSI interface	AVDD12_CSI
CSI2A_L1N	R5	AIO	CSI interface	AVDD12_CSI
CSI2A_L2P	U4	AIO	CSI interface	AVDD12_CSI
CSI2A_L2N	U3	AIO	CSI interface	AVDD12_CSI
CSI2B_L0P	V2	AIO	CSI interface	AVDD12_CSI
CSI2B_L0N	V1	AIO	CSI interface	AVDD12_CSI
CSI2B_L1P	V4	AIO	CSI interface	AVDD12_CSI
CSI2B_L1N	V3	AIO	CSI interface	AVDD12_CSI
SSUSB				
SSUSB_RXN	J27	AIO	SSUSB RXDATA	AVDD12_SSUSB
SSUSB_RXP	H27	AIO	SSUSB RXDATA	AVDD12_SSUSB
SSUSB_TXN	J24	AIO	SSUSB TXDATA	AVDD12_SSUSB
SSUSB_TXP	J25	AIO	SSUSB TXDATA	AVDD12_SSUSB
WBG				
XIN_WBG	H8	AIO	WBG crystal clock input	AVDD18_WBG
WF_IN	C1	AIO	Wifi I channel negative-end	AVDD18_WBG
WF_IP	B1	AIO	Wifi I channel positive-end	AVDD18_WBG
WF_QN	D2	AIO	Wifi Q channel negative-end	AVDD18_WBG
WF_QP	D1	AIO	Wifi Q channel positive-end	AVDD18_WBG
BT_IN	F1	AIO	BT I channel negative-end	AVDD18_WBG
BT_IP	F2	AIO	BT I channel positive-end	AVDD18_WBG
BT_QN	G2	AIO	BT Q channel negative-end	AVDD18_WBG
BT_QP	G1	AIO	BT Q channel positive-end	AVDD18_WBG
GPS_I	J2	AIO	GPS I channel	AVDD18_WBG
GPS_Q	J1	AIO	GPS Q channel	AVDD18_WBG
USB				
USB_DM	F26	AIO	USB D+ differential data line	AVDD33_USB
USB_DP	G26	AIO	USB D- differential data line	AVDD33_USB
CHD_DM	G24	AIO	BC1.1 charger DP	AVDD33_USB
CHD_DP	G25	AIO	BC1.1 charger DM	AVDD33_USB
UFS				

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Pin name	Pin no.	Type	Description	Power domain
UFS_CKIN_26M	F23	AIO	26MHz clock input for UFS	AVDD18_UFS
UFS_TX0_P	B24	AIO	UFS interface	AVDD18_UFS
UFS_TX0_N	A24	AIO	UFS interface	AVDD18_UFS
UFS_RX0_RXP	A22	AIO	UFS interface	AVDD18_UFS
UFS_RX0_RXN	B22	AIO	UFS interface	AVDD18_UFS
UFS_RST_N	E22	AIO	UFS interface	AVDD18_UFS
General purpose				
PERIPHERAL_EN0	R25	DIO	PERIPHERAL_EN0	DVDD18
PERIPHERAL_EN1	L25	DIO	PERIPHERAL_EN1	DVDD18
PERIPHERAL_EN2	M22	DIO	PERIPHERAL_EN2	DVDD18
PERIPHERAL_EN3	L22	DIO	PERIPHERAL_EN3	DVDD18
PERIPHERAL_EN4	Y25	DIO	PERIPHERAL_EN4	DVDD18
PERIPHERAL_EN5	AD25	DIO	PERIPHERAL_EN5	DVDD18
PERIPHERAL_EN6	N22	DIO	PERIPHERAL_EN6	DVDD18
PERIPHERAL_EN7	T22	DIO	PERIPHERAL_EN7	DVDD18
PERIPHERAL_EN8	K22	DIO	PERIPHERAL_EN8	DVDD18
PERIPHERAL_EN9	V22	DIO	PERIPHERAL_EN9	DVDD18
PERIPHERAL_EN10	Y7	DIO	PERIPHERAL_EN10	DVDD18
PERIPHERAL_EN11	Y6	DIO	PERIPHERAL_EN11	DVDD18
PERIPHERAL_EN12	AD22	DIO	PERIPHERAL_EN12	DVDD18
PERIPHERAL_EN13	AD19	DIO	PERIPHERAL_EN13	DVDD18
PERIPHERAL_EN14	AA7	DIO	PERIPHERAL_EN14	DVDD18
MISC				
DRVBUS	AF26	DIO	This signal enables to drive 5V on Vbus. 0: Not drive Vbus 1: Drive 5V on Vbus	DVDD18
IDDIG	AF23	DIO	Indicates whether the connected plug is a mini-A or mini-B 0: Connected plug is a mini-A (ID is connected to GND). 1: Connected plug is a mini-B (ID is floating).	DVDD18
TN_PLLGP1	Y12	AIO	Reserved	
TP_PLLGP1	Y13	AIO	Reserved	
Analog power				
AVDD04_DSI	V27	P	Analog power for DSI	-
AVDD09_SSUSB	K27	P	Analog power for SSUSB	-
AVDD09_UFS	C22	P	Analog power for UFS	-
AVDD12_CSI	W3	P	Analog power for CSI	-
AVDD12_DSI	V23	P	Analog power for DSI	-
AVDD12_MD	AH20	P	Analog power for modem	-
AVDD12_PLLGP	AA13	P	Analog power for PLL	-
AVDD12_UFS	C23	P	Analog power for UFS	-
AVDD12_USB	H22	P	Analog power for USB	-

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Pin name	Pin no.	Type	Description	Power domain
AVDD12_WBG	C2	P	Analog power for WBG	-
AVDD18_AP	AH21	P	Analog power input 1.8V	-
AVDD18_CPU	AC7	P	Analog power input 1.8V for CPU	-
AVDD18_DDR	G9	P	Analog power input 1.8V for DRAM	-
AVDD18_MD	AH19	P	Analog power input 1.8V for modem	-
AVDD18_PLLGP	AB13	P	Analog power input 1.8V for PLL	-
AVDD18_SSUSB	H23	P	Analog power input 1.8V for SSUSB	-
AVDD18_UFS	D23	P	Analog power 1.8V for UFS	-
AVDD18_USB	F27	P	Analog power 1.8V for USB	-
AVDD18_WBG	B2	P	Analog power 1.8V for WBG (Wi-Fi, BT, GPS)	-
AVDD2_EMI	G18	P	DRAM power	-
AVDD2_EMI	H11	P	DRAM power	-
AVDD2_EMI	H13	P	DRAM power	-
AVDD2_EMI	H16	P	DRAM power	-
AVDD33_USB	F25	P	Analog power 3.3V for USB	-
AVDDQ_EMI	G14	P	DRAM power	-
AVDDQ_EMI	G15	P	DRAM power	-
AVDDQ_EMI	H10	P	DRAM power	-
AVDDQ_EMI	H12	P	DRAM power	-
AVDDQ_EMI	H17	P	DRAM power	-
AVDDQ_EMI	H19	P	DRAM power	-
Digital power				
DVDD_CORE	H21, ...	P	Digital power input for Vcore	-
DVDD_GPU	J19, ...	P	Digital power input for GPU	-
DVDD_MODEM	AA15, ...	P	Digital power input for LTE	-
DVDD_PROC_B	AA10, ...	P	Digital power input for Big Core	-
DVDD_PROC_L	U7, ...	P	Digital power input for Little Core	-
DVDD_SRAM_CORE	J12, ...	P	Digital power input for Vcore SRAM	-
DVDD_SRAM_GPU	T18, ...	P	Digital power input for GPU SRAM	-
DVDD_SRAM_PROC_B	AC13	P	Digital power input for Big Core SRAM	
DVDD_SRAM_PROC_L	W7	P	Digital power input for Little Core SRAM	
DVDD18_IOLT	M27	P	Digital power input for IO (region 1)	-
DVDD18_IOLM	W27	P	Digital power input for IO (region 2)	-
DVDD18_IOBL	AJ21	P	Digital power input for IO (region 3)	-
DVDD18_IORB	AA1	P	Digital power input for IO (region 4)	-
DVDD18_IORT	L2	P	Digital power input for IO (region 5)	-
DVDD18_MSDC0	E27	P	Digital power input for MSDC0	-
DVDD18_MSDC1	AA27	P	Digital power input for MSDC1	-
DVDD28_MSDC1	AB27	P	Digital power input for MSDC1	
DVDD18_SIM	AG27	P	Digital power input for SIM1/2	-
DVDD28_SIM1	AF25	P	Digital power input for SIM1	-

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Pin name	Pin no.	Type	Description	Power domain
DVDD28_SIM2	AE27	P	Digital power input for SIM2	-
ESD				
CDM3P5A	AF7	G	Analog ground input for modem	-
CDM5P5A	AE7	G	Analog ground input for WBG	-
Digital ground				
DVSS	A21, ...	G		-

Table 2-5. Acronym for table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

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2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-6. Absolute maximum ratings for power supply

Symbol or pin name	Description	Max.	Unit
AVDD04_DSI	Analog power	0.84	V
AVDD09_SSUSB	Analog power	0.99	V
AVDD09_UFS	Analog power	0.99	V
AVDD12_CSI	Analog power	1.32	V
AVDD12_DSI	Analog power	1.32	V
AVDD12_MD	Analog power	1.32	V
AVDD12_PLLGP	Analog power	1.32	V
AVDD12_UFS	Analog power	1.32	V
AVDD12_USB	Analog power	1.32	V
AVDD12_WBG	Analog power	1.32	V
AVDD18_AP	Analog power	1.98	V
AVDD18_CPU	Analog power	1.98	V
AVDD18_DDR	Analog power	1.98	V
AVDD18_MD	Analog power	1.98	V
AVDD18_PLLGP	Analog power	1.98	V
AVDD18_SSUSB	Analog power	1.98	V
AVDD18_UFS	Analog power	1.98	V
AVDD18_USB	Analog power	1.98	V
AVDD18_WBG	Analog power	1.98	V
AVDD2_EMI	Analog power (LP4) Analog power (LP3)	1.17 1.3	V
AVDD33_USB	Analog power	3.22	V
AVDDQ_EMI	Analog power (LP4) Analog power (LP3)	0.63 1.3	V
DVDD18_IOLT DVDD18_IOLM DVDD18_IOBL DVDD18_IORB DVDD18_IORT	Digital power input for 1.8V IO	1.98	V
DVDD18_MSDC0	Digital power input for MSDC0	1. 95	V
DVDD18_MSDC1	Digital power input for MSDC1	1. 95	V
DVDD28_MSDC1	Digital power input for MSDC1	3.3	V
DVDD28_SIM1	Digital power input for SIM1	3.3	V
DVDD28_SIM2	Digital power input for SIM2	3.3	V
DVDD_CORE	Digital power input for CORE	0.84	V
DVDD_GPU	Digital power input for GPU	0.95	V
DVDD_PROC_B	Digital power input for Big Core	1.18	V
DVDD_PROC_L	Digital power input for Little Core	1.18	V

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Symbol or pin name	Description	Max.	Unit
DVDD_MODEM	Digital power input for MODEM	0.79	V
DVDD_SRAM_CORE	Digital power input for Vcore SRAM	0.95	V
DVDD_SRAM_GPU	Digital power input for GPU	1.05	V
DVDD_SRAM_PROC_B	Digital power input for Big Core	1.18	V
DVDD_SRAM_PROC_L	Digital power input for Little Core	1.18	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

2.2.2 Recommended Operating Conditions

Table 2-7. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD04_DSI	Analog power	0.67	0.7	0.74	V
		0.76	0.8	0.84	V
AVDD09_SSUSB	Analog power	0.86	0.9	0.94	V
AVDD09_UFS	Analog power	0.86	0.9	0.94	V
AVDD12_CSI	Analog power	1.14	1.2	1.26	V
AVDD12_DSI	Analog power	1.14	1.2	1.26	V
AVDD12_MD	Analog power	1.14	1.2	1.26	V
AVDD12_PLLGP	Analog power	1.14	1.2	1.26	V
AVDD12_UFS	Analog power	1.14	1.2	1.26	V
AVDD12_USB	Analog power	1.14	1.2	1.26	V
AVDD12_WBG	Analog power	1.14	1.2	1.26	V
AVDD18_AP	Analog power	1.71	1.8	1.89	V
AVDD18_CPU	Analog power	1.71	1.8	1.89	V
AVDD18_DDR	Analog power	1.71	1.8	1.89	V
AVDD18_MD	Analog power	1.71	1.8	1.89	V
AVDD18_PLLGP	Analog power	1.71	1.8	1.89	V
AVDD18_SSUSB	Analog power	1.71	1.8	1.89	V
AVDD18_UFS	Analog power	1.71	1.8	1.89	V
AVDD18_USB	Analog power	1.71	1.8	1.89	V
AVDD18_WBG	Analog power	1.71	1.8	1.89	V
AVDD33_USB	Analog power	2.92	3.07	3.22	V
AVDD2_EMI	Analog power (LP4)	1.06	1.1	1.17	V
	Analog power (LP3)	1.14	1.2	1.30	
AVDDQ_EMI	Analog power (LP4)	0.57	0.6	0.63	V
	Analog power (LP3)	1.14	1.2	1.30	
DVDD18_IOLT DVDD18_IOLM DVDD18_IOBL DVDD18_IORB DVDD18_IORT	Digital power input for 1.8V IO	1.62	1.8	1.98	V

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Symbol or pin name	Description	Min.	Typ.	Max.	Unit
DVDD18_MSDC0	Digital power input for MSDC0	1.70	1.8	1.95	V
DVDD18_MSDC1	Digital power input for MSDC1	1.70	1.8	1.95	V
DVDD28_MC1	Digital power input for MSDC1	2.70	3	3.30	V
DVDD28_SIM1	Digital power input for SIM1	2.70	3	3.30	V
DVDD28_SIM2	Digital power input for SIM2	2.70	3	3.30	V
DVDD_CORE	Digital power input for CORE (0.6V is only for idle state)	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
DVDD_GPU	Digital power input for GPU	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
		0.86	0.9	0.95	V
DVDD_PROC_B	Digital power input for Big Core	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
		0.90	0.95	1.00	V
		1.06	1.12	1.18	V
DVDD_PROC_L	Digital power input for Little Core	0.57	0.6	0.63	V
		0.67	0.7	0.74	V
		0.76	0.8	0.84	V
		0.90	0.95	1.00	V
		1.06	1.12	1.18	V
DVDD_MODEM	Digital power input for MODEM (0.55V is only for idle state)	0.52	0.55	0.58	V
		0.62	0.65	0.68	V
		0.67	0.7	0.74	V
		0.71	0.75	0.79	V
DVDD_SRAM_CORE	Digital power input for Vcore SRAM (0.6V is only for idle state)	0.57	0.6	0.63	V
		0.86	0.9	0.95	V
DVDD_SRAM_GPU	Digital power input for GPU	0.81	0.85	0.89	V
		0.86	0.9	0.95	V
		0.95	1	1.05	V
DVDD_SRAM_PROC_B	Digital power input for Big Core SRAM	0.86	0.9	0.95	V
		1.00	1.05	1.10	V
		1.06	1.12	1.18	V
DVDD_SRAM_PROC_L	Digital power input for Little Core SRAM	0.86	0.9	0.95	V
		1.00	1.05	1.10	V
		1.06	1.12	1.18	V

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2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 DC Electrical Characteristics

2.2.4.1 RTC DC Electrical Characteristics

Table 2-8. RTC DC electrical characteristics (DVDD18_IOLT =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLT		DVDD18_IOLT + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLT	V
VOH	DC output logic low voltage	0.75*DVDD18_IOLT			V
VOL	DC output logic high voltage			0.25*DVDD18_IOLT	V
FRTC	Input clock frequency		32		kHz
DCRTC	Input signal duty cycle	45	50	55	%

2.2.4.2 SPI, I2S DC Electrical Characteristics

Table 2-9. SPI, I2S DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOH	DC output logic low voltage	0.75*DVDD18_IORB			V
VOL	DC Output logic high voltage			0.25*DVDD18_IORB	V

2.2.4.3 I2C0, I2C1, I2C2 DC Electrical Characteristics

Table 2-10. I2C0, I2C1, I2C2 DC electrical characteristics (DVDD18_IORB =1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IORB		DVDD18_IORB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IORB	V
VOL	DC output logic high voltage			0.2*DVDD18_IORB	V

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2.2.4.4 I2C3 DC Electrical Characteristics

Table 2-11. I2C3 DC electrical characteristics (DVDD18_IOLB =1.8V)

Parameters	Descriptions	Min.	Typ	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD18_IOLB		DVDD18_IOLB + 0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD18_IOLB	V
VOL	DC output logic high voltage			0.2*DVDD18_IOLB	V

2.2.4.5 MSDC0 DC Electrical Characteristics

Table 2-12. MSDC0 DC electrical characteristics (DVDD28_MSDC0=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.65*DVDD28_MSDC0		DVDD28_MSDC0+0.3	V
VIL	Input logic high voltage	-0.3		0.35*DVDD28_MSDC0	V
VOH	DC output logic low voltage	1.4			V
VOL	DC output logic high voltage			0.45	V

2.2.4.6 MSDC1 DC Electrical Characteristics

Table 2-13. MSDC1 DC electrical characteristics (DVDD28_MSDC1=2.8V/3.3V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	0.625* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.25* DVDD28_MSDC1	V
VOH	DC output logic low voltage	0.75* DVDD28_MSDC1		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.125* DVDD28_MSDC1	V

Table 2-14. MSDC1 DC electrical characteristics (DVDD28_MSDC1=1.8V)

Parameters	Descriptions	Min.	Typ.	Max.	Unit
VIH	Input logic low voltage	1.27		DVDD28_MSDC1 + 0.3	V
VIL	Input logic high voltage	-0.3		0.58	V
VOH	DC output logic low voltage	1.4		DVDD28_MSDC1 + 0.3	V
VOL	DC output logic high voltage	-0.3		0.45	V

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2.2.4.7 SIM DC Electrical Characteristics

Table 2-15. SIM DC electrical characteristics

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SIO						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SCLK						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM1_SRST						
Input high voltage	DVDD28_SIM1 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM1 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
SIM2_SIO						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.4	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.27	V
Input high voltage	DVDD28_SIM2= 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.6	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SCLK						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V

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Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.22	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.4	V
SIM2_SRST						
Input high voltage	DVDD28_SIM2 = 1.8V	V_{ih}	1.4	1.8	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.27	V
Output high voltage		V_{oh}	1.62	1.8	1.9	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V
Input high voltage	DVDD28_SIM2 = 3.0V	V_{ih}	2.6	3.0	N/A	V
Input low voltage		V_{il}	N/A	0.0	0.4	V
Output high voltage		V_{oh}	2.7	3.0	3.1	V
Output low voltage		V_{ol}	N/A	0.0	0.36	V

2.2.5 AC Electrical Characteristics and Timing Diagram

2.2.5.1 External Memory Interface for LPDDR3

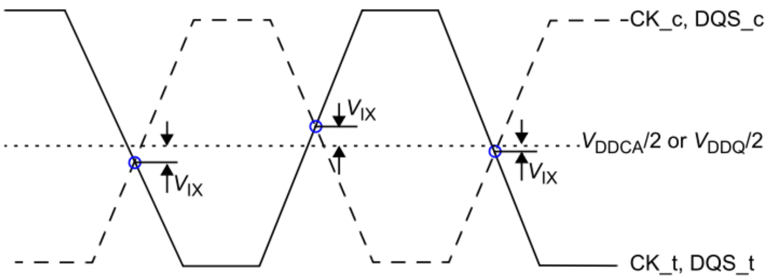

Figure 2-3. LPDDR3 VIX definition

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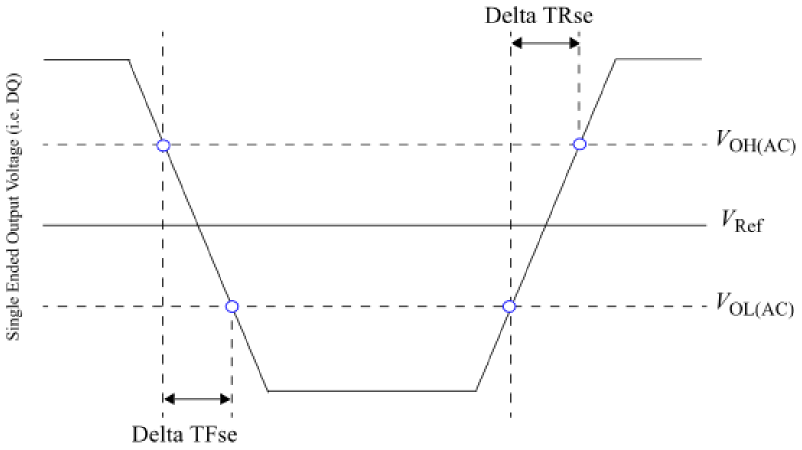

Figure 2-4. LPDDR3 single-ended output slew-rate definition

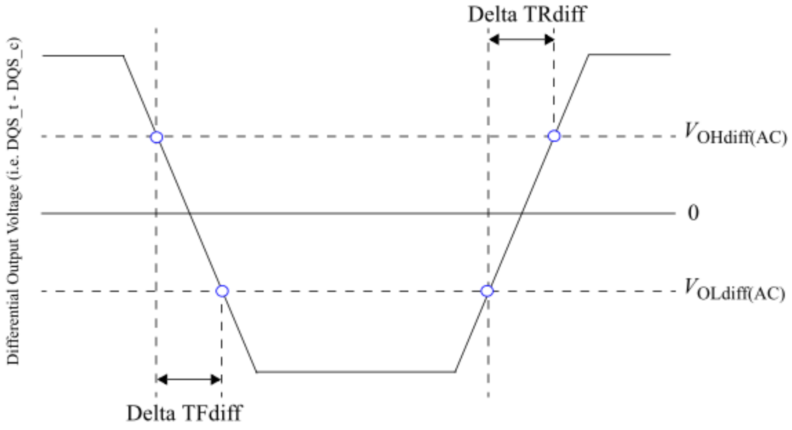

Figure 2-5. LPDDR3 differential output slew-rate definition

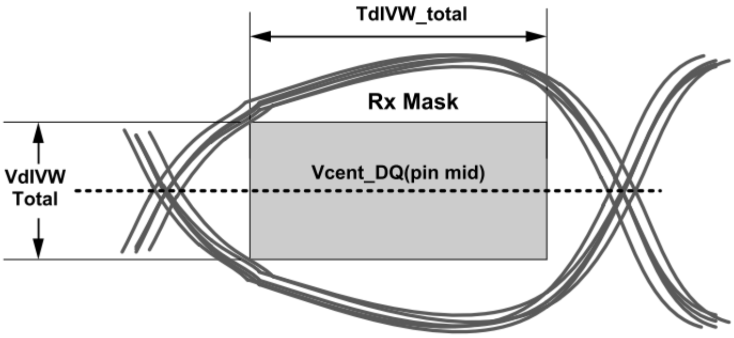

Figure 2-6. LPDDR3 RX mask

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Table 2-16. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
VIXCA	Differential input cross point voltage relative to VDDCA/2 for CK_t, CK_c	-120		120	mV
VIXDQ	Differential input cross point voltage relative to VDDQ/2 for DQS_t, DQS_c	-120		120	mV
SRQse	Single-ended output slew rate (RON = 40Ω +/-30%)	1.5		4	V/ns
SRQdiff	Differential output slew rate (RON = 40Ω +/-30%)	3		8	V/ns
VdIVW_total	Rx mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)			0.25	UI

2.2.5.2 External Memory Interface for LPDDR4/LPDDR4X

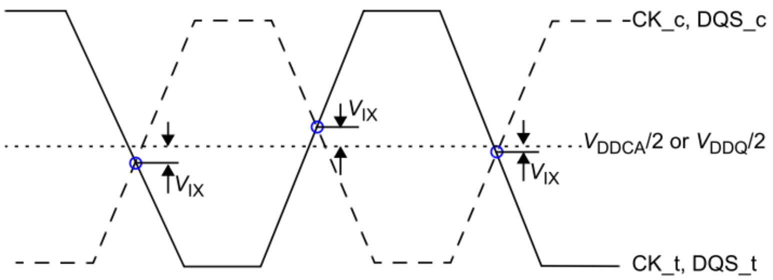

Figure 2-7. LPDDR4/LPDDR4X VIX definition

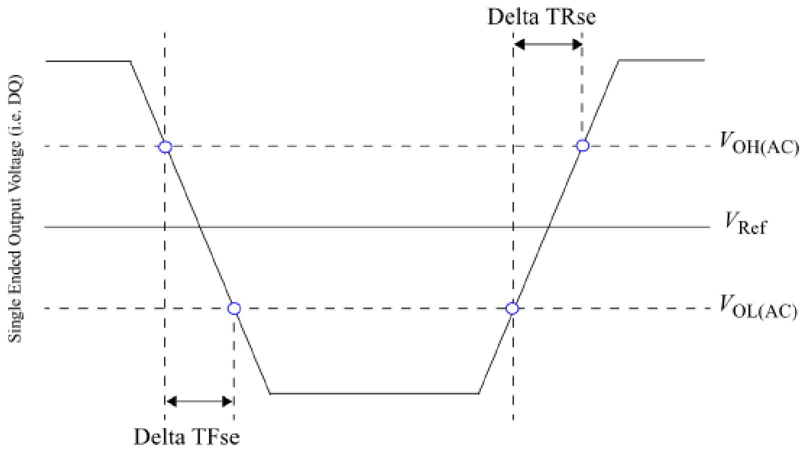

Figure 2-8. LPDDR4/LPDDR4X single-ended output slew-rate definition

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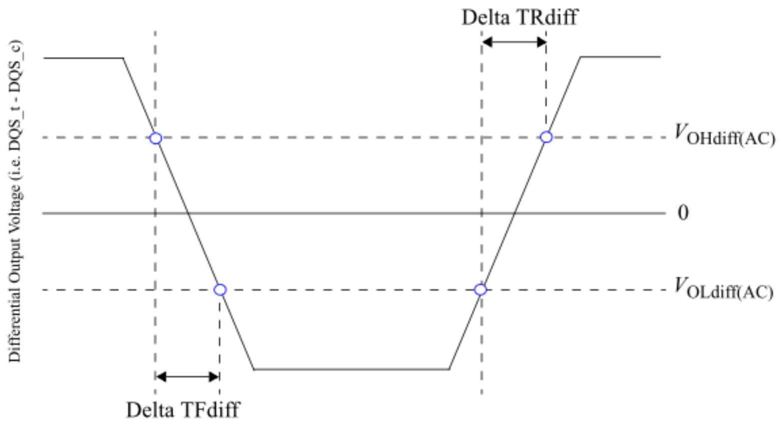

Figure 2-9. LPDDR4/LPDDR4X differential output slew-rate definition

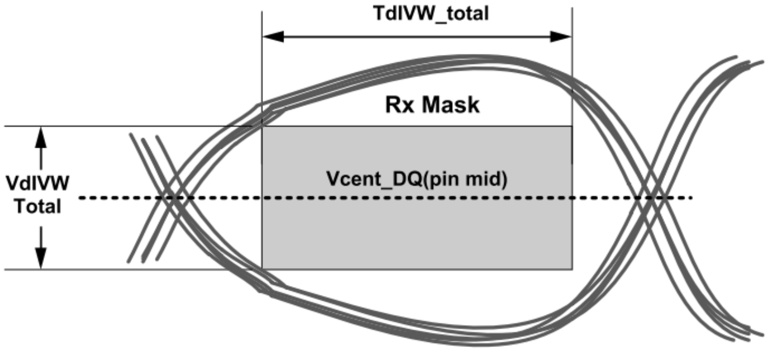

Figure 2-10. LPDDR4/LPDDR4X RX mask

Table 2-17. LPDDR4/LPDDR4X AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
Vix_DQS_ratio	DQS differential input crosspoint voltage ratio			20	%
Vix_CK_ratio	CK differential input crosspoint voltage ratio			25	%
SRQse (LPDDR4)	Single-ended output slew rate	3.5		9	V/ns
SRQse (LPDDR4X)	Single-ended output slew rate	3		9	V/ns
SRQdiff (LPDDR4)	Differential output slew rate	7		18	V/ns
SRQdiff (LPDDR4X)	Differential output slew rate	6		18	V/ns
VdIVW_total	Rx Mask voltage - p-p total			140	mV
TdIVW_total	Rx timing window total (at VdIVW voltage levels)			0.25	UI

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2.2.5.3 SPI AC Timing Characteristics

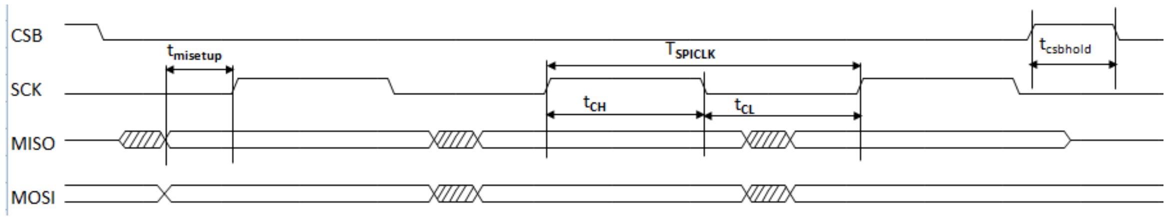

Figure 2-11. SPI timing diagram

Table 2-18. SPI AC timing parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI clock period	T_{SPICLK}	18.2	-	-	Ns
SPI clock low time	t_{CL}	9.1	-	-	Ns
SPI clock high time	t_{CH}	9.1	-	-	Ns
SPI CSB hold time	$t_{csbhold}$	9.1	-	-	Ns
SPI MISO setup time (MISO 80%, SCK 20%)	$t_{misetup}$	28.5	-	-	Ns

2.2.5.4 I2S AC Timing Characteristics

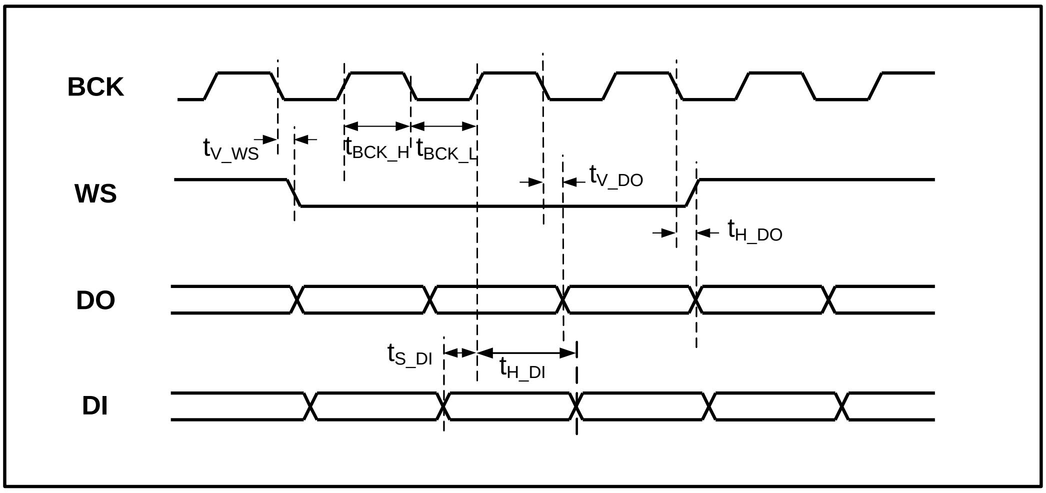

Figure 2-12. I2S master mode timing diagram

Table 2-19. I2S AC timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
f_S	Sampling frequency	8	-	192	kHz
t_{WS}	Word select period	32	-	64	$1/f_{BCK}$
f_{MCK}	Master clock frequency	-	-	24.576	MHz

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Parameter	Description	Min.	Typ.	Max.	Unit
f_{BCK}	Serial clock frequency	32 * f_S	-	64 * f_S	MHz
t_{BCK_H}	BCK high-level time	-	0.5	-	$1/f_{BCK}$
t_{BCK_L}	BCK low-level time	-	0.5	-	$1/f_{BCK}$
t_{V_WS}	WS valid time	-	-	0.2	$1/f_{BCK}$
t_{H_WS}	WS hold time	0	-	-	$1/f_{BCK}$
t_{V_DO}	DO valid time	-	-	0.2	$1/f_{BCK}$
t_{H_DO}	DO hold time	0	-	-	$1/f_{BCK}$
t_{S_DI}	DI setup time	0.2	-	-	$1/f_{BCK}$
t_{H_DI}	DI hold time	0.2	-	-	$1/f_{BCK}$

2.2.5.5 I2C AC Timing Characteristics

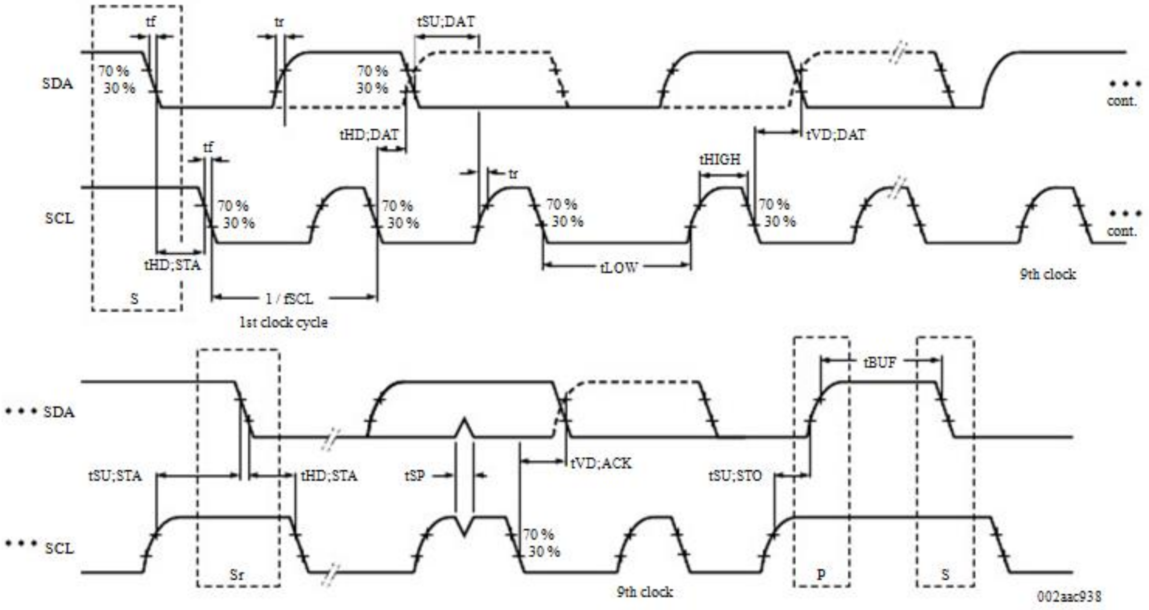

Figure 2-13. I2C timing diagram of standard mode (100kHz) and fast mode (400kHz)

Table 2-20. I2C AC timing parameters

Symbol	Standard mode	Fast mode	Unit	Note
$t_{HD;STA}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration register.
t_{LOW}	5	1.25	µs	
t_{HIGH}	5	1.25	µs	
$t_{SU;STA}$	2.5	0.625	µs	
$t_{HD;DAT}$	2.5	0.625	µs	
$t_{SU;DAT}$	2.5	0.625	µs	
$t_{SU;STO}$	2.5	0.625	µs	Can be extended by 0x28, extension configuration

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Symbol	Standard mode	Fast mode	Unit	Note
				register.

2.2.5.6 MSDC AC Timing Characteristics

2.2.5.6.1 Default Speed Timing

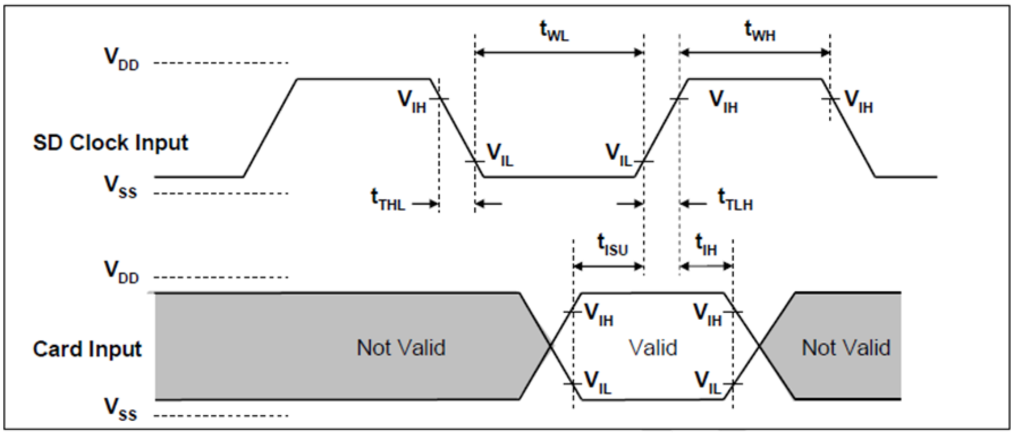

Figure 2-14. MSDC device input timing diagram of default speed

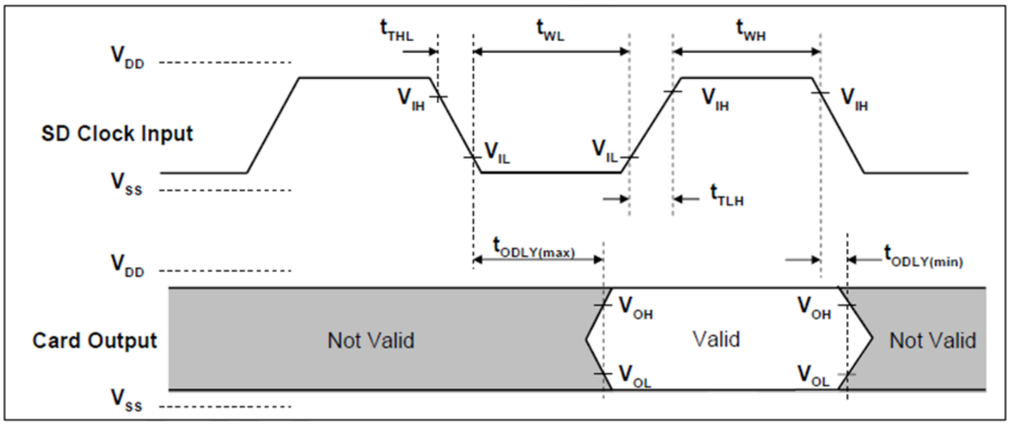

Figure 2-15. MSDC device output timing diagram of default speed

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Table 2-21. MSDC device AC timing parameters of default speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	25	MHz	C_{CARD}≦10pF (1 card)
Clock frequency identification mode	f_{OD}	0(1) / 100	400	kHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	10		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	T_{ISU}	5		ns	C_{CARD}≦10pF (1 card)
Input hold time	T_{IH}	5		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	T_{ODLY}	0	14	ns	C_L≦40pF (1 card)
Output delay time during identification mode	T_{ODLY}	0	50	ns	C_L≦40pF (1 card)

2.2.5.6.2 High Speed Timing

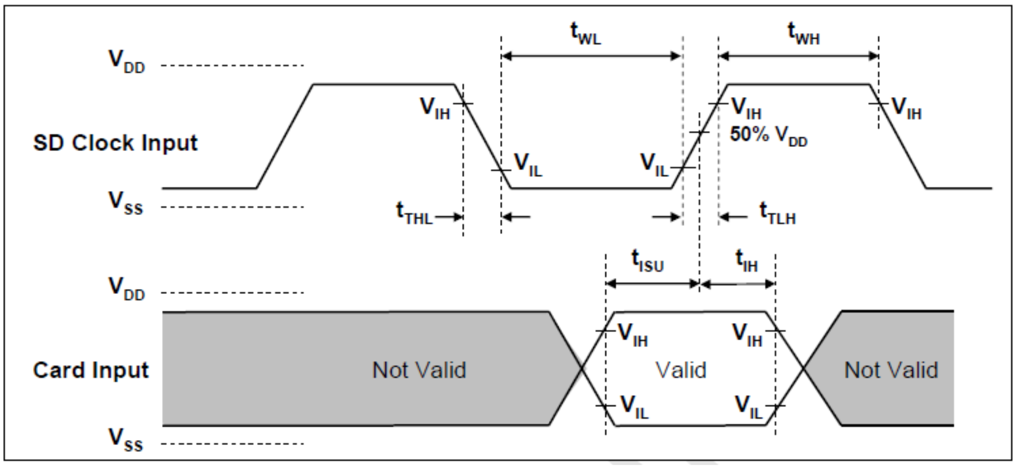

Figure 2-16. MSDC device input timing diagram of high speed

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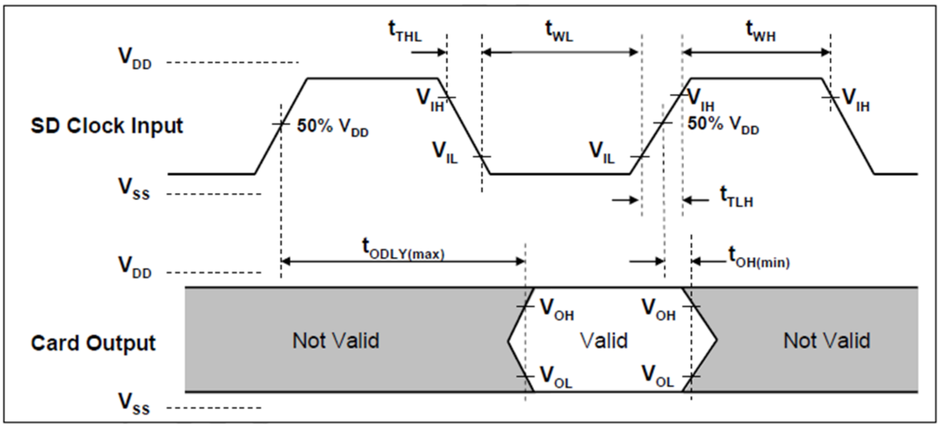

Figure 2-17. MSDC device output timing diagram of high speed

Table 2-22. MSDC device AC timing parameters of high speed

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}))					
Clock frequency data transfer mode	f_{PP}	0	50	MHz	C_{CARD}≦10pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD}≦10pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD}≦10pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD}≦10pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD}≦10pF (1 card)
Input CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD}≦10pF (1 card)
Output CMD, DAT (referenced to CLK)					
Output delay time during data transfer mode	t_{ODLY}		14	ns	C_L≦40pF (1 card)
Output hold time	t_{OH}	2.5		ns	C_L≧15pF (1 card)
Total system capacitance for each line	C_L		40	pF	1 card

2.2.5.6.3 SDR12/SDR25/SDR50/SDR104 Mode Timing

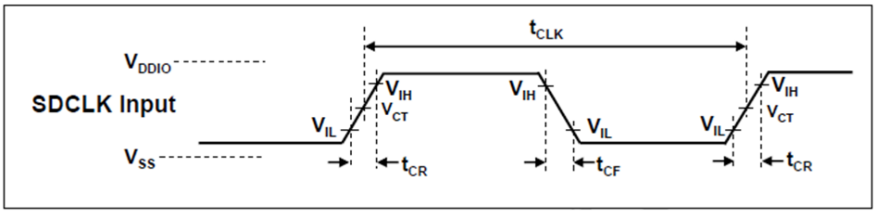

Figure 2-18. MSDC device clock timing diagram of SDR12/SDR25/SDR50/SDR104 mode

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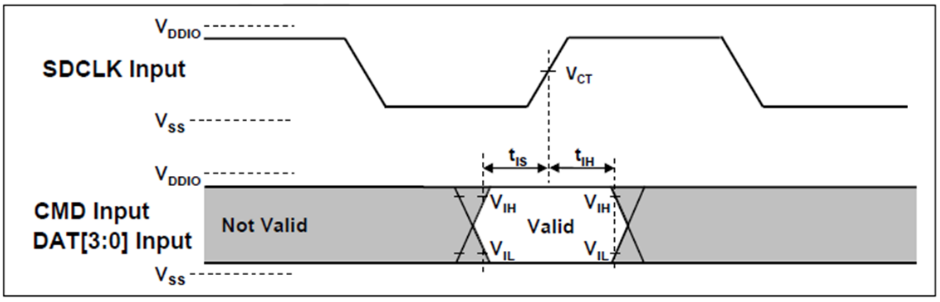

Figure 2-19. MSDC device input timing diagram of SDR50/SDR104 mode

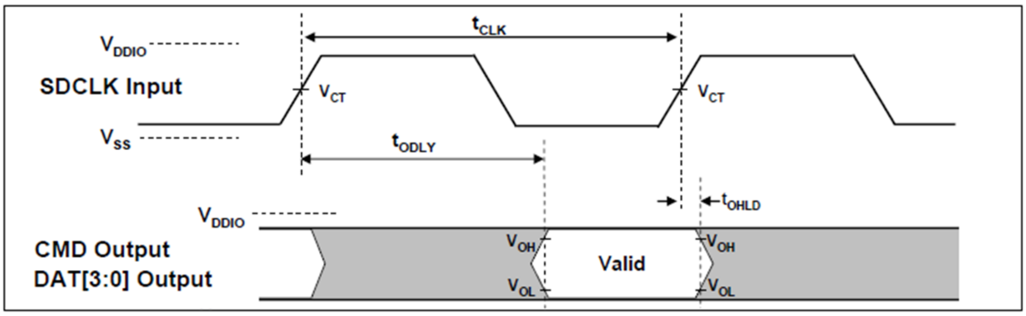

Figure 2-20. MSDC device output timing diagram of fixed data window (SDR12/SDR25/SDR50)

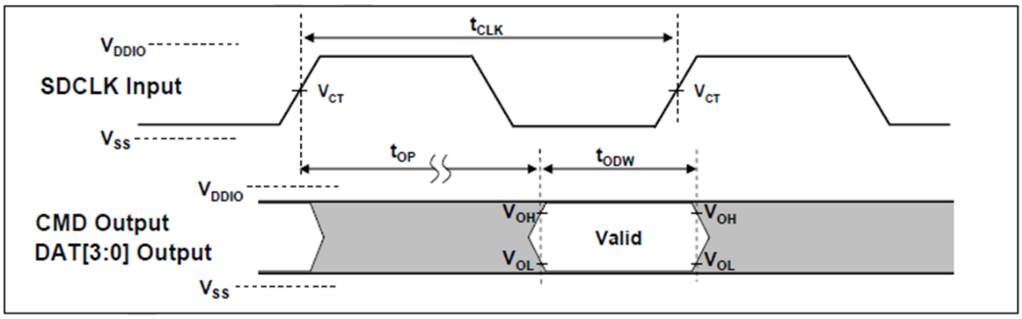

Figure 2-21. MSDC device output timing diagram of variable window (SDR104)

Table 2-23. MSDC device AC timing parameters of SDR12/SDR25/SDR50/SDR104 mode

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{CLK}	4.8	-	ns	208MHz (Max), Between rising edge, V_{CT}=0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.

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Symbol	Min.	Max.	Unit	Remark
Clock Duty	30	70	%	
Input CMD, DAT (SDR104)				
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}=0.975V
Input CMD, DAT (SDR50)				
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}=0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}=0.975V
Output CMD, DAT (SDR12/SDR25/SDR50)				
t_{ODLY}	-	7.5	ns	t_{CLK}≧10.0ns, C_L=30pF, using driver type B, for SDR50
t_{ODLY}		14	Ns	t_{CLK}≧20.0ns, C_L=40pF, using driver type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min), C_L=15pF
Output CMD, DAT (SDR104)				
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay varioation due to temperature change after tunung.
t_{ODW}	0.6	-	UI	t_{ODW}=2.88ns at 208MHz

2.2.5.6.4 DDR50 Speed Mode Timing

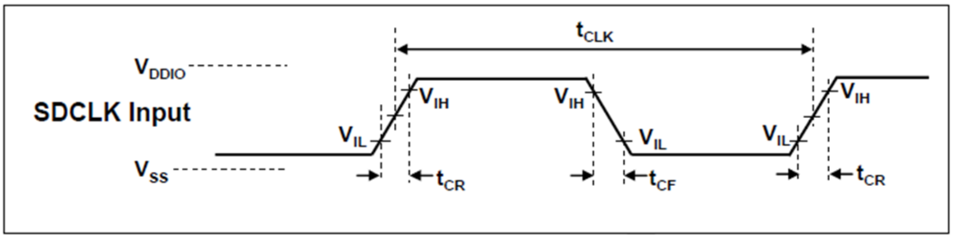

Figure 2-22. MSDC device clock timing diagram of DDR50 speed mode

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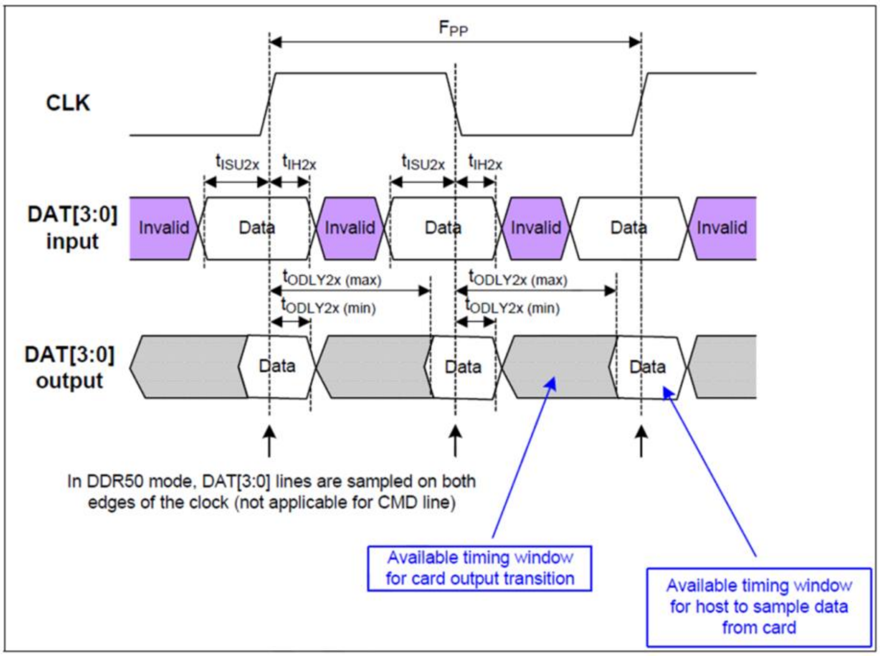

Figure 2-23. MSDC device input/output timing diagram of DDR50 speed mode

Table 2-24. MSDC device AC timing parameters of DDR50 speed mode

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	6	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output delay time during data transfer mode	t_{ODLY}	-	13.7	ns	C_L≦30pF (1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L≧15pF (1 card)
Input DAT (referenced to CLK rising and falling edge)					
Input setup time	t_{ISU}	3	-	ns	C_{CARD}≦10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD}≦10pF (1 card)
Output DAT (referenced to CLK rising and falling edge)					
Output delay time during data transfer mode	t_{ODLY}	-	7.0	ns	C_L≦25pF (1 card)
Output hold time	t_{OH}	1.5	-	Ns	C_L≧15pF (1 card)

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2.2.5.6.5 HS200 Speed Timing

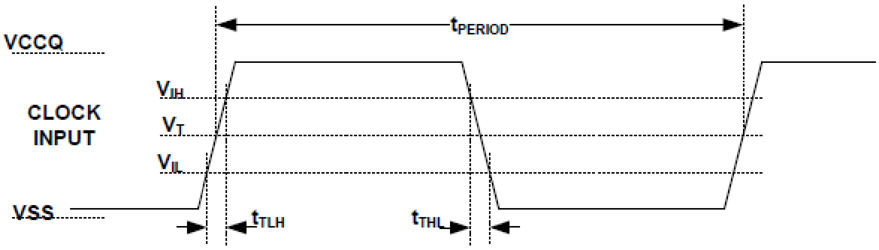
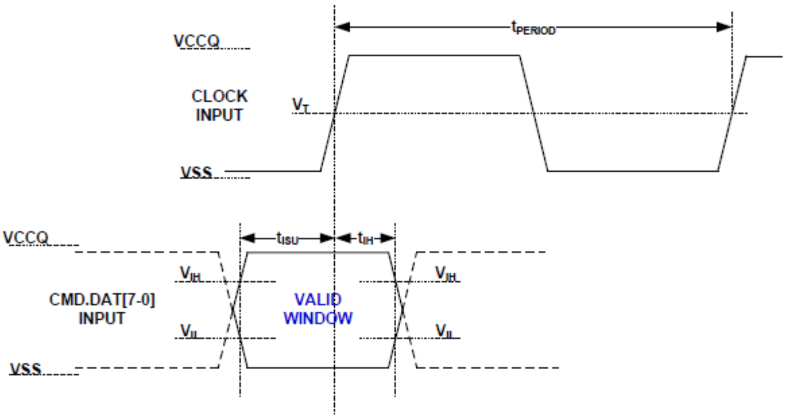


Figure 2-24. MSDC device clock timing diagram of HS200



NOTE 1 t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
NOTE 2 V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 2-25. MSDC device input timing diagram of HS200

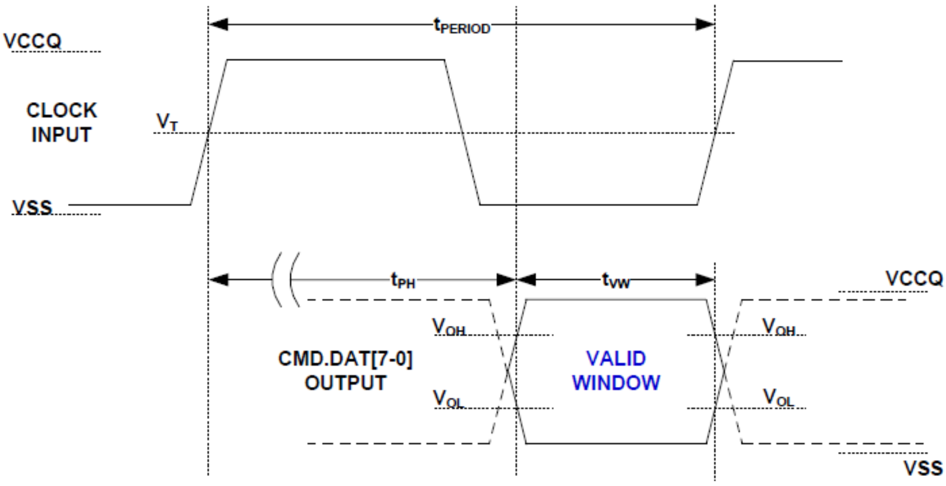


Figure 2-26. MSDC device output timing diagram of HS200

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Table 2-25. MSDC device AC timing parameters of HS200

Symbol	Min.	Max.	Unit	Remark
Clock CLK				
t_{PERIOD}	5	-	ns	200MHz (max.), between rising edge
t_{TLH}, t_{THL}	-	0.2 * t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{DEVICE}=6pF The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	
Input CMD, DAT				
t_{ISU}	1.40	-	ns	$C_{DEVICE} \leqq$ 6pF
t_{IH}	0.80		ns	$C_{DEVICE} \leqq$ 6pF
Output CMD, DAT				
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20℃)	+1550 (ΔT=90℃)	ps	Delay variation due to temperature change after tunung. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
t_{VW}	0.575	-	UI	t_{VW}=2.88ns at 208MHz
Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

2.2.5.6.6 HS400 Speed Timing

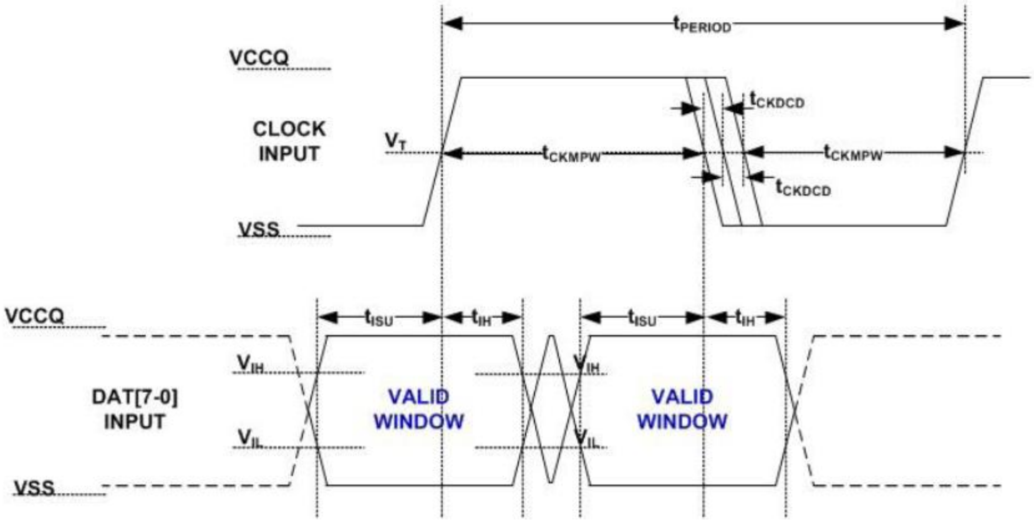

Figure 2-27. MSDC device input timing diagram of HS400

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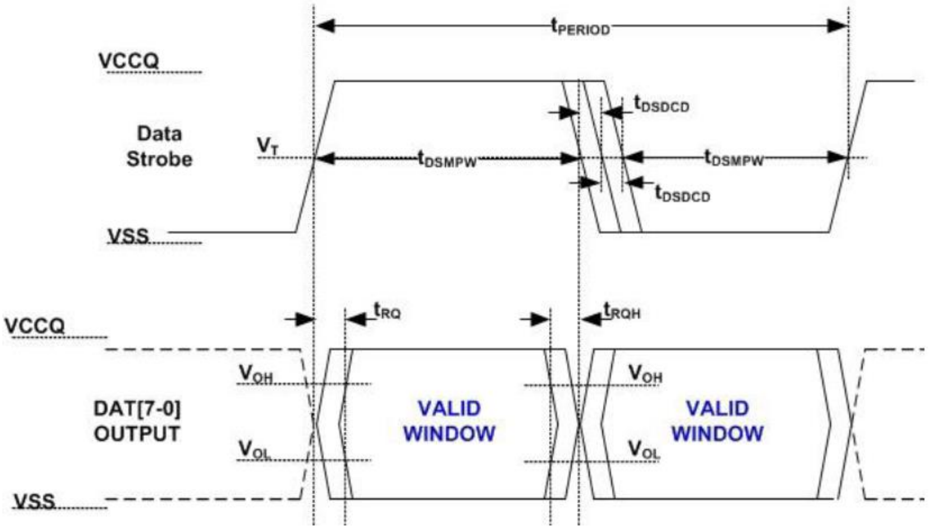

Figure 2-28. MSDC device output timing diagram of HS400

Table 2-26. MSDC device AC timing parameters of HS400

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input setup time	t_{ISUddr}	0.4		ns	$C_{Device} \leqq 6pF$. With respect to V_{IH}/V_{IL}
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leqq 6pF$. With respect to V_{IH}/V_{IL}
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5		ns	200MHz (max.), between rising edges. With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T.
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is valid.
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max. value is specified by manufacturer. Value up to infinite is

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Parameter	Symbol	Min.	Max.	Unit	Remark
					valid.
Input DAT (referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

2.2.5.7 SIM AC Timing Characteristics

Table 2-27. SIM AC timing parameters

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
SIM1_SCLK						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	50	Ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM1_SIO						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM1_SRST						
Rise and fall time	DVDD28_SIM1 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM1 = 3.0V	T_{rise_fall}	N/A	18	1000	ns
SIM2_SCLK						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	50	ns
Clock duty		Duty	47	50	53	%
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	18	ns
Clock duty		Duty	47	50	53	%
SIM2_SIO						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	50	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	50	1000	ns
SIM2_SRST						
Rise and fall time	DVDD28_SIM2 = 1.8V	T_{rise_fall}	N/A	18	1000	ns
Rise and fall time	DVDD28_SIM2 = 3.0V	T_{rise_fall}	N/A	18	1000	ns

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2.3 System Configuration

2.3.1 Mode Selection

Table 2-28. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)
[0] AUD_DAT_MOSI0 [1] PWRAP_SPI0_CSN	00: Use SPI pin for legacy JTAG, DPI pin for IO_JTAG 01: Use MSDC1 pins for legacy JTAG 10: No dedicate JTAG 11: Use SPI pin for legacy JTAG
[0] AUD_DAT_MISO0	0: NA (default) 1: DP/DM output JTAG
[0] AUD_DAT_MISO1	0: eMMC booting 1: UFS booting
[0] PWRAP_SPI0_MI [0] PWRAP_SPI0_MO	00: LPDDR3 01: LPDDR4 10: LPDDR4X 11: LPDDR4X+

2.3.2 Constant Tie Pins

Table 2-29. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

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2.4 Power-on Sequence

The power-on/off sequence is shown in the following figure:

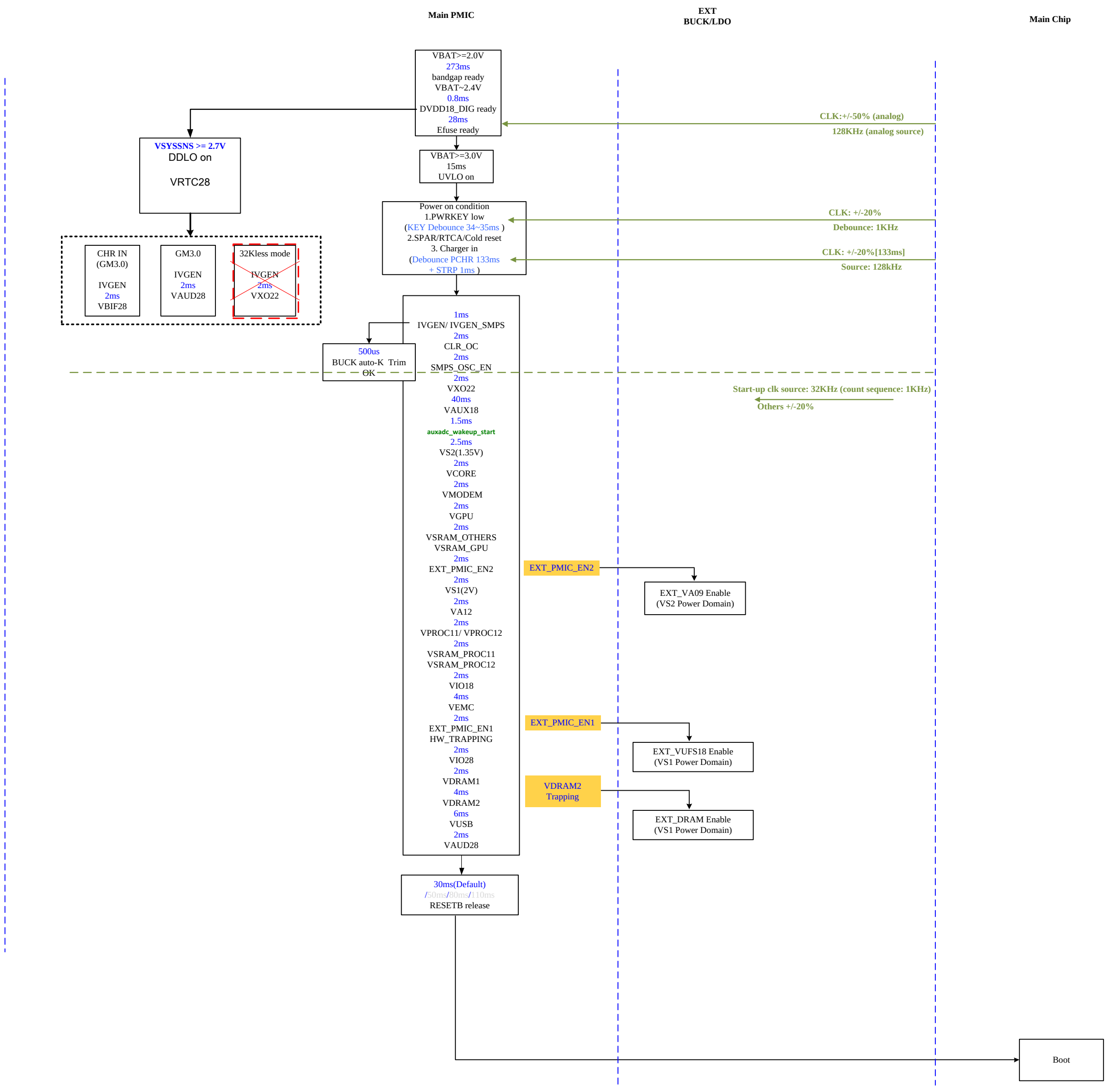

Figure 2-29. Power-on sequence

Refer to PMIC datasheet for detailed timing sequence.

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2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- DETADC: An ADC that detects calibration, thermal data from RF chip.
- RF control: A DAC for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers.
- Auxiliary ADC: Provides an ADC for auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA base-band signal processing:

- BBRX
- BBTX
- ETDAC
- DETADC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

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A/D converter: 12 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

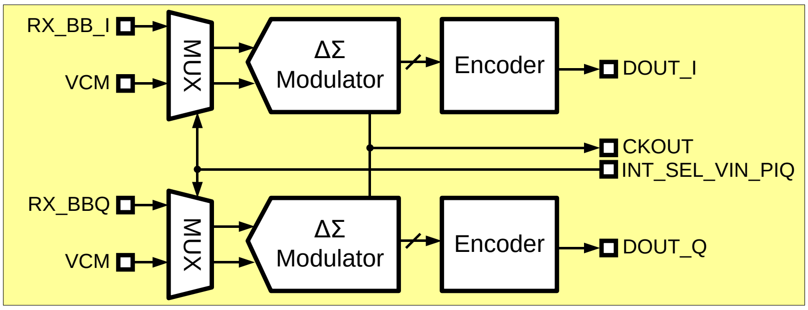

Figure 2-30. Block diagram of BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-30. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (peak-to-peak)			1.2	V
VCM	Common mode input voltage	0.65	0.7	0.75	V
RIN	Input resistance	2.8		7.0	kΩ
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C

2.5.3.2 BBTX

2.5.3.2.1 Block Descriptions

Each BBTX includes two channel DACs with the 1st order low pass filter.

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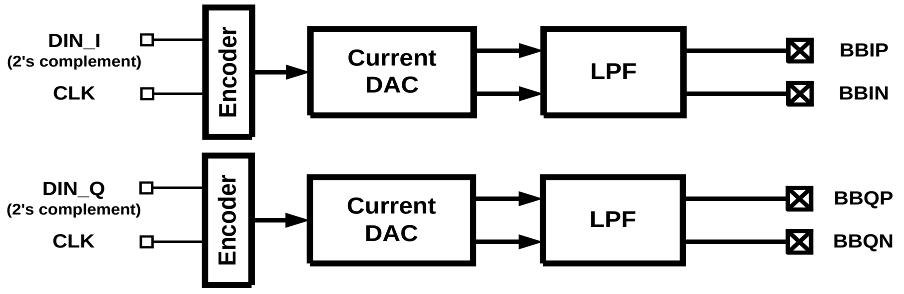

Figure 2-31. Block diagram of BBTX

2.5.3.2.2 Functional Specifications

Table 2-31. BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
V_{fs}	DAC output swing		2100		mV
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C

2.5.3.3 ETDAC

2.5.3.3.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. D/A converter: Converts digital modulated signals to analog domain.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 1st-order filter frequency response.

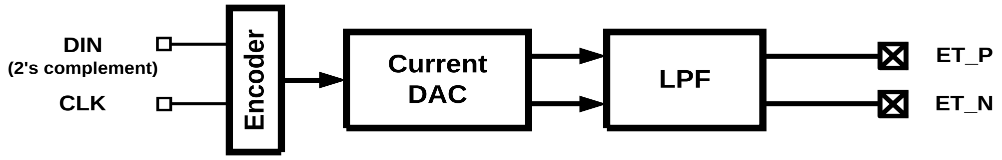

Figure 2-32. Block diagram of ETDAC

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2.5.3.3.2 Functional Specfications

Table 2-32. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
VOCM	Output CM voltage	0.615	0.65	0.685	V
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C

2.5.3.4 DETADC

2.5.3.4.1 Block Descriptions

The DETADC (DETection ADC) performs I/Q-channel path detections from RF chip:

1. Input buffer: For each channel, isolates RF signals from high-speed ADCs.
2. A/D converters: Convert the detected signals to digital data.

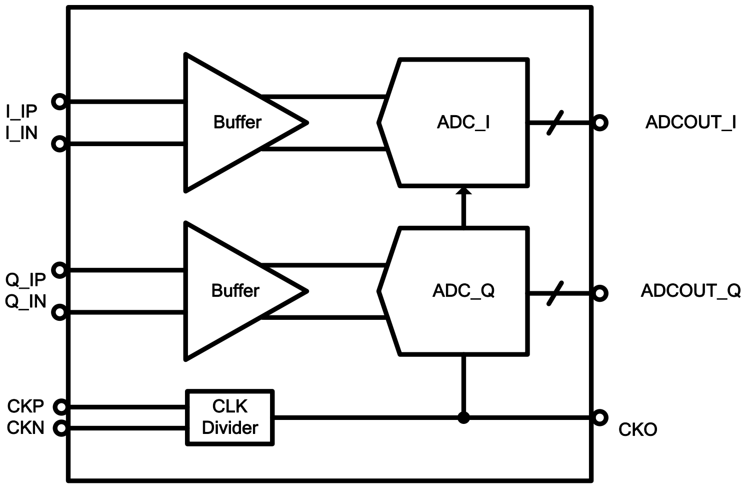

Figure 2-33. Block diagram of DETADC

2.5.3.4.2 Functional Specifications

See the table below for the functional specifications of DETADC

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Table 2-33. DETADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Analog input voltage (differential peak-to-peak)		1.2		V
VCM	Common mode input voltage		0.55		V
RIN	Input resistance	1.6	2	2.4	kΩ
CIN	Input capacitance		2	3	pF
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		80	°C

2.5.3.5 APC-DAC

2.5.3.5.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin.

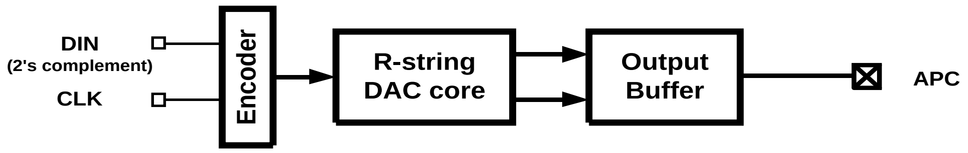

Figure 2-34. Block diagram of APC-DAC

2.5.3.5.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC.

Table 2-34. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
F_S	Clock rate	1.0833		2.1666	MS/s
T_S	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD – 0.2	V
C_L	Output loading capacitance		220	2200	pF
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	−20		85	°C

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2.5.3.6 AUXADC

2.5.3.6.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

Table 2-35. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)
Channel 1	External use (AUX_IN1)
Channel 2	External use (AUX_IN2)
Channel 3	External use (AUX_IN3)
Channel 4	External use (AUX_IN4)
Channel 5~15	NA

2.5.3.6.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-36. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		3.25/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel (PAD loading excluded)		 50 4		 fF pF
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Accuracy			+-10	mV

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2.5.3.7 Clock Squarer

2.5.3.7.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-37. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Vin	Input signal amplitude	400	800	1,200	mVpp
	Maximum Positive Overshoot			1.32	V
	Minimum Negative Overshoot	-0.1			V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C

2.5.3.8 Temperature Sensor

2.5.3.8.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-38. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C

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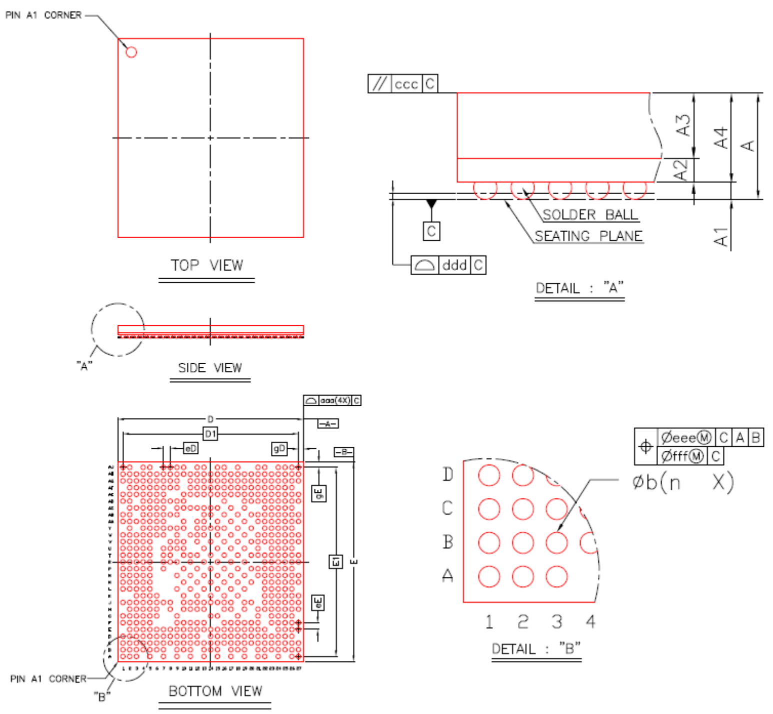
2.6 Package Information

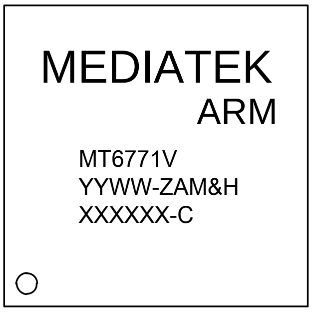
2.6.1 Package Outlines



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	10.9	11.0	11.1
	Y	E	11.7	11.8	11.9
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.141 Ref.		
Substrate+Mold Thickness		A4	0.541	0.591	0.641
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.14	0.18	0.22
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	599		
Edge Ball Center to Center	X	D1	10.40		
	Y	E1	11.20		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

Figure 2-35. Outlines and dimensions of VFBGA 11mm*11.8mm, 599-ball, 0.9mm pitch package

2.6.2 Top Marking Definition



MT6771A : Part No
YYWW : Data Code
& : Subcontractor Code
XXXXX : Die Lot No

Figure 2-36. Top marking of MT6771V/C

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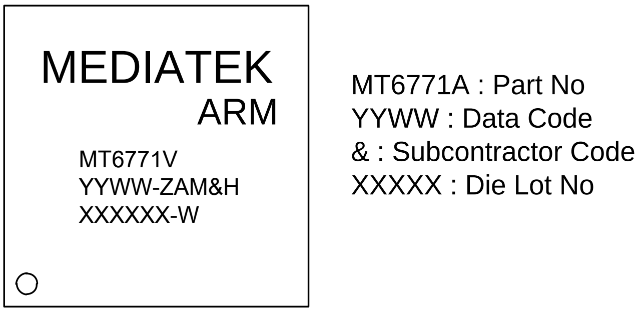

Figure 2-37. Top marking of MT6771V/W

2.6.3 Thermal Operating Specifications

Table 2-39. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	37.65	°C/Watt	

2.6.4 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

2.6.5 MSL

MSL of this chip is 3.

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